1-13-2016

Melting and Crystallization of Si and Ge2Sb2Te5 Nanostructures

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Adam Cywar, Ph.D.

University of Connecticut, 2016

Recent technological advances in fabrication processes have allowed for the production of solid-state devices with dimensions as small as ~10 nm. Improving the functionality and efficiency of these devices must come from new technologies and fabrication processes. In this work, two device technologies which are driven by the thermal processes of melting and crystallization are studied in detail. A novel oscillator device concept is explored in which a Si micro-/nanowire exhibits relaxation oscillations as it switches between solid and liquid phases, resulting in large amplitude current pulses. Phase change memory (PCM), a non-volatile memory technology that shows promising scaling and performance to compete with flash memory technology, is also studied through modeling of device performance and a critical fabrication process step.

This dissertation demonstrates the interesting phenomenon of a nanoscale Si solid-liquid phase-change oscillator and pulse generator, and that the frequency can be controlled or tuned by various parameters as is demonstrated experimentally and verified with simulations. Simulation results also suggest that the devices have strong scalability into the nanometer scale as electrical breakdown of silicon is expected to be a significant factor, allowing for faster melting of the nanowire and oscillation frequencies >1 GHz.

Electrical performance of PCM devices with various geometries and load conditions is analyzed using finite element modeling with temperature dependent parameters, demonstrating the impact of load conditions and incremental geometry

variations. This dissertation also discusses a model for crystallization of $Ge_2Sb_2Te_5$ (GST) which is able to simulate the crystallization of an arbitrarily shaped GST nanostructure during any annealing conditions or electrical device operation, developed in collaboration with fellow group member Zachary Woods. A model for void formation is developed and incorporated into the crystallization model, as voids occur during crystallization due to the density change between amorphous and crystalline phases. This model offers the utility of capturing the nanoscale phenomena of incubation, nucleation, growth and void formation in GST, and closely agrees with various experiments performed at IBM and elsewhere in the literature.

Melting and Crystallization of Si and $Ge_2Sb_2Te_5$ Nanostructures

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B.S., University of Connecticut, **2010**

A Dissertation

Submitted in Partial Fulfillment of the

Requirements for the Degree of

Doctor of Philosophy

at the

University of Connecticut

2016

APPROVAL PAGE

Doctor of Philosophy Dissertation

Melting and Crystallization of Si and $Ge_2Sb_2Te_5$ Nanostructures

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2016

Acknowledgements

I would like to thank my advisors, Prof. Ali Gokirmak and Prof. Helena Silva for their mentorship and guidance during my Ph.D. I would also like to thank Prof. Rajeev Bansal and Prof. Radenka Maric for being on my advisory committee and instructing me in their excellent graduate courses.

I would like to thank Dr. Chung Lam at IBM for giving me the opportunity to collaborate with the phase-change memory group at the Watson Research Center, and SangBum Kim, Norma Sosa and Matt Brightsky for helpful discussions and advice on my project. I would also like to thank Yu Zhu and Armand Galan for their helpful advice and favors regarding the device fabrication at IBM, and also Jing Li for advice on the device performance simulations.

I would like to thank my former and current labmates; accordingly I thank Nicholas Williams for the comradery at UConn from undergraduate throughout our entire Ph.D. careers, Azer Faraclas, Zachary Woods, Niaz Khan and Sean Fischer for the fun times shared together both in and out of the lab, Jacob Scoggin for taking over device fabrication duties from me at IBM, Kadir Cil, Sadid Muneer and Lhacene Adnane for being so kind and helpful to me in the lab, Gokhan Bakan, Mustafa Akbulut and Faruk Dirisaglik for setting an example of a successfully graduating Ph.D. student, and Nafisa Noor, Nadim Kanan, Abdiel Rivera, Luca Lucera, Akan Peng, Nabila Adnane, Zoila Jurado, Lindsay Sullivan, Jon Rarey and Sencer Ayas for being great team members.

I would also like to acknowledge the sources of my funding and support: the National Science Foundation for the Graduate Research Fellowship Program award, the Department of Education for the Graduate Assistantship in Areas of National Need

award, IBM for the internship and collaboration, and the University of Connecticut for the Teaching Assistantship and Research Assistantship.

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1. Introduction

1.1 Nanocrystalline/amorphous Si thin films and structures

Large area-electronics such as flat panel displays, x-ray imaging arrays and solar cells commonly use amorphous silicon (a-Si) and nanocrystalline silicon (nc-Si) for thin film devices due to their uniformity and ease of production in low-temperature processing, despite their low electrical carrier mobility which results in excessive power consumption. There is considerable interest in achieving TFTs with high carrier mobility, which would enable high performance circuitry with flat panel displays and sensor arrays as complete systems on glass or plastic. This has motivated studies over the recent decades [1-3] on the crystallization of a-Si and nc-Si. a-Si can be annealed to achieve polycrystalline silicon (poly-Si) which has a much higher carrier mobility, however the temperature required for this is too high to be compatible with low-temperature substrates such as glass and plastic. We investigate a novel crystallization technique of nanocrystalline silicon (nc-Si) microstructures by self-heating and melting the structures with high current densities (~20 MA/cm^2) for short durations (~1 μs), allowing for growth from melt upon resolidification [4], shown in Figure 1.1. This rapid self-heating technique offers the advantage of locally heating the thin film Si structures, enabling their crystallization without damaging the substrate.

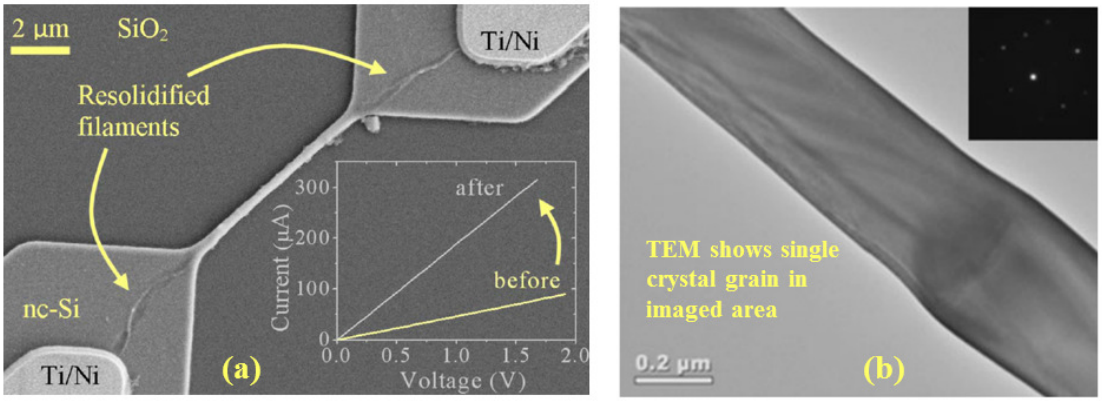


Figure 1.1 (a) nc-Si microwire crystallized from melt via self-heating technique, with I-V characteristics shown before and after the anneal (inset). (b) TEM showing a large single crystal grain in a Si microwire that is crystallized from melt via self-heating, with the diffraction pattern shown (inset) [4].

Experiments on melting and crystallization of nanocrystalline Si microwires through self-heating are performed using various pulsing methods such as high-amplitude rectangular or triangular voltage pulse, repeated rectangular pulsing with finely incrementing amplitude, and pulsing through a load resistor with parallel capacitance. High voltage rectangular pulses are useful to observe the electrical characteristics of the wire in the liquid state, however it is not a reliable method for crystallizing the wires as there is nothing to limit the power to the wires due to the positive feedback nature of the self-heating since the resistivity of Si in liquid state is drastically reduced. Using a triangular pulse or using repeated pulses with finely incrementing amplitude are more reliable methods to obtain a crystallized wire. Implementing a load resistor and parallel capacitance can self-limit the power to the wire once it melts and reduce the power after crystallization if the load resistance used is somewhere between the initial high resistance and the final low resistance. However, this can lead to relaxation oscillations.

1.2 Oscillators

The need for local clocks within a chip due to the large number of devices and power dissipation problem has increased demand for low cost, low power, compact, and high-speed oscillator circuits, resulting in significant advances in the two current alternative technologies to crystal oscillators: MEMS (micro-electro-mechanical structures) oscillators and CMOS oscillators. Both types of oscillators are now used in a wide variety of applications including telecommunications and wireless networks in which the crystals' highest frequency accuracy (<0.1 ppm) is not required [5, 6].

MEMS based oscillators can have quality factors comparable to crystal oscillators and their processing is suitable for low cost mass production, making them advantageous for some applications. MEMS resonators, despite the moving parts, are also highly resistant to shock and vibrations due to their small size and mass. However, it is challenging to achieve low power operation at high frequencies (>100 MHz) due to increased motional resistance [7].

CMOS based oscillators are integrated circuits that make use of feedback loops with variable, large capacitors or inductors and field-effect or bipolar transistors. These are fully compatible with the logic and memory chip and have no moving parts, hence are expected to have higher reliability. Their main disadvantage is the relatively poor frequency accuracy (100 ppm) due to fabrication process, voltage noise and especially the operation temperature variation. They also consume large chip areas, on the order of 500 x 500 μm^2 [8-13] but compared to off-chip crystal or MEMS alternatives this is only a minor drawback. Both MEMS and CMOS oscillator technologies are expected to

replace crystal oscillators in an increasing number of applications, but both still face significant challenges.

Rapid solid–liquid phase-change oscillations are observed [14, 15] in nanocrystalline silicon (nc-Si) microwires while investigating crystal growth from melt at micrometer scale through rapid self-heating [4, 16], as mentioned in section 1.1. High amplitude relaxation oscillations in current (2–20 mA) through a single Si microwire are observed when the wire is placed in parallel with a capacitor and is biased through a load resistor that has approximately equal resistance to the crystallized wire (Figure 1.2). Experimental oscillation frequencies are on the order of 1–10 MHz. In a relaxation oscillator, voltage in the capacitor increases until the upper threshold of the switching element is reached, at which point the switching element toggles and discharges the capacitor, lowering the voltage below the lower threshold of the switching element and toggling it back, thus oscillation occurs. Finite element modeling is performed to compare to the experiments, and also study the scalability and frequency limitations of this phenomenon by simulating scenarios with smaller wires with lesser capacitance than those used in the experiments. An oscillator device concept based on these solid-liquid oscillations is expected to have substantial power density as they can pass a significant amount of current and the devices can fabricated in a very small area ($< 10\ \mu m^2$), much smaller than typical CMOS and MEMS oscillators. The devices are also expected to be suitable for high-temperature applications where conventional CMOS technology cannot operate, as the phase-change oscillator operates via a thermally driven process.

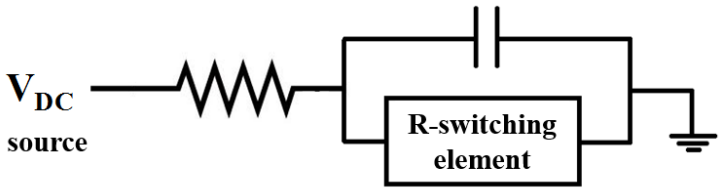


Figure 1.2 A simple circuit schematic of a relxation oscillator comprised of a DC voltage source, a resistor, and a capacitor in parallel with a resistance switching element.

1.3 Phase change memory

Phase change memory (PCM) has become a technology of interest for non-volatile memory over the past 15 years. The concept of PCM originated in the 1960s, however it only recently has been considered viable for storage class memory due to the improvements in fabrication technology and materials engineering [17]. PCM is a resistive memory technology, where a '1' or '0' is represented by a low-resistance state or high-resistance state in the device. Billions of write and erase cycles are achieved by using a chalcogenide glass such as $Ge_2Sb_2Te_5$ (GST) which can repeatedly and rapidly change phase between crystalline (low-resistance) and amorphous (high-resistance) states [17]. Changing the material from crystalline to amorphous state (reset) requires melting and rapid freezing of a small volume of the material such that the atoms do not have time to arrange in a crystalline fashion. Reversing the phase back to crystalline state from amorphous state (set) requires heating the material above its crystallization temperature for a sufficient time so that the atoms rearrange themselves in crystalline order (Figure 1.3). The timescale for a reset operation is in the order of ~ 10 ns, and is in the order of ~ 100 ns for a set operation. PCM shows promising results for device scaling into the

nanometer scale as reduced dimensions result in lower power and current requirements, as well as higher packing density and higher speed of operation [18].

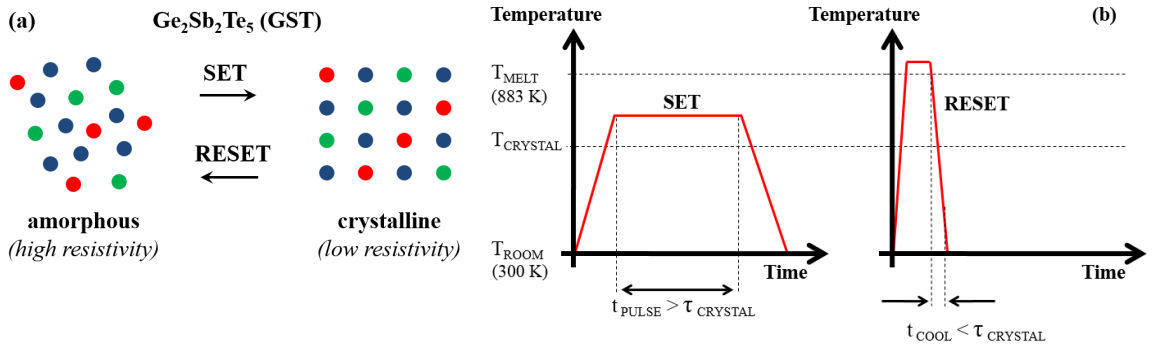


Figure 1.3 (a) Diagram to illustrate difference in molecular structure between amorphous and crystalline GST, with arrows drawn to show the direction of programming operations. Actual molecular structures can be seen in Ref. [19]. (b) Temperature–time characteristics for the programming operations [17].

There is considerable interest in studying and modeling phase transitions and device operation in GST PCM cells for the development of phase-change memory technology [17, 18], as there are three phase transitions that take place (amorphous to crystalline, crystalline to liquid, and liquid to amorphous). The importance of using temperature dependent material parameters in the finite element modeling of a reset operation is demonstrated, capturing the non-linear current-time (and thus temperature-time) characteristics that occur during the crystalline to liquid phase transition and show the impact of the non-linear behavior for various load conditions and geometries. However, the amorphous to crystalline phase transition is of the most interest as it is has additional complexity in the phenomena of nucleation and growth of crystal grains in an

amorphous matrix, and is important for understanding the set operation as well as fabrication processing techniques.

There are several advanced crystallization models reported in the literature [20-22] that simulate nucleation and growth of crystal grains in GST, however these very sophisticated models have limited flexibility to be incorporated into simulations of device operation or fabrication process steps. A flexible crystallization model for nucleation and growth in GST is developed in collaboration with fellow group member Zachary Woods, building upon his existing framework which models the fractional crystallinity in a local area using an effective media approach. This flexible model can simulate crystallization of GST via nucleation and growth in any structure or device geometry under arbitrary heating conditions where a thermal gradient and/or a transient may be present. Simulations performed in COMSOL Multiphysics enable this crystallization model to be compatible alongside any other physics such as joule heating and solid mechanics. This approach allows for the modeling of crystallization during a set/reset operation or a fabrication process step, allowing for material properties to be dynamically updated and applied to areas that are constantly changing shape in the simulation, which can be otherwise be very difficult in a finite element model with static domains.

The current models for the crystallization of GST reported in the literature do not account for the ~ 6.5% volume reduction that occurs upon the as-deposited amorphous to crystalline phase change. Experimental results have shown that a confined volume of as-deposited amorphous GST typically exhibits one or more voids after crystallization during annealing. The locations and sizes of the resulting voids are critically important to the quality of the device performance. Modeling the volume change and void formation

during crystallization to predict void locations and sizes will significantly help with designing experiments for determining the most optimum process conditions and device geometry. Cutting down the number of experiments by having a more careful experimental design can save a significant amount time and costs associated with device fabrication. A model that captures the volume change and void formation in GST upon crystallization is demonstrated in this dissertation.

2. Phase change oscillations in Si microwires

2.1 Annealing of Si microwires

In the crystallization experiments, as-fabricated wires are nanocrystalline/ amorphous mixed phase with a negative temperature coefficient of resistance (TCR) (Figure 2.1(a)). Sufficiently high currents (20 MA/cm^2) forced through the wires lead to self-heating and melting [23]. The melting temperature of bulk Si is 1415 °C [24] and the resistivity of liquid Si is $7x10^{-5}$ Ω-cm [4, 24, 25], approximately two orders of magnitude lower than the wires' room temperature resistivity. The self-heating process in conjunction with the wire's negative TCR results in positive feedback – wire resistance (R_W) decreases as joule heating increases, causing an increase in dissipated power ($P_{wire} = V_{wire}^2 / R_W$) leading to a thermal runaway and melting. The self-heating process cannot be controlled if a constant voltage pulse is applied directly to the wire since there is no load to limit P_{wire}, resulting in melting and breaking of the wire. Figure 2.1(b) shows four distinct regions of I-t characteristics during self-heating due to a constant voltage pulse. Region 1 is the transient period corresponding to voltage ramp. In regions 2 and 3 the increase in current can be attributed to thermal carrier generation, annealing of wire defects, dopant activation, and growth of nanocrystal size [2, 26]. The increase in current in region 4 is due to melting, and the wire is completely molten when current reaches a plateau. The wire breaks and stops conducting at the end of region 4. Many of these measurements of pulsing and melting wires have contributed to the calculation of liquid resistivity of Si using a wafer-level technique [4].

Applying a triangular voltage pulse to the wire is a more controllable method of annealing since P_{wire} is forced to decrease by the ramp down in voltage (Figure 2.1(c)).

Wires which fully melt during high current stresses have positive TCR in lower temperature range and four to ten times lower resistances after stress (R_{WF}) than their as-fabricated resistances (R_{W0}) (Figure 2.1(d)), indicating a change in the phase of the Si. After a completely melted and crystallized, further improvement in its room temperature conductivity saturates (Figure 2.2). However, if an already crystallized wire is heated but not melted, wire resistance can be increased up to 50% of R_{W0} [2]. This is attributed to formation of fractures as well as concentration of dopants into the grains during resolidification and diffusion of dopants from the grains to the grain boundaries during lower temperature annealing [2]. These annealing processes are used in resistance trimming of heavily doped polycrystalline silicon resistors [1]. Another more controllable method of crystallizing a wire is to deliver repeated pulses to a wire, starting from a low voltage that does not affect the wire and incrementing the voltage by a small amount (100 mV) with each pulse. Wire resistance during and after each pulse can be monitored, which shows the critical points where permanent changes in the wire happen. Results of this method are shown in Figure 2.2. LABVIEW controls for the measurement equipment in these experiments are shown in Appendix 8.1.

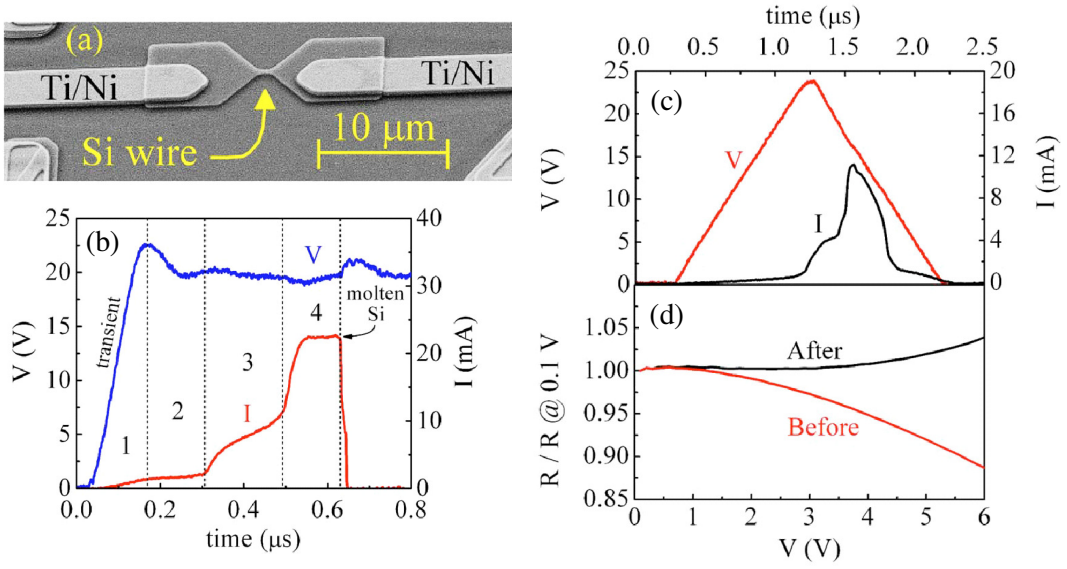


Figure 2.1 (a) SEM of an as-fabricated Si microwire. (b) I-t characteristics of a wire during a rectangular voltage pulse, and (c) for a triangular voltage pulse. (d) Scaled resistance before and after the triangular pulse, demonstrating the change in temperature coefficient of resistance. Resistance before the triangular pulse = 51.4 kΩ, resistance after the pulse = 4.7 kΩ.

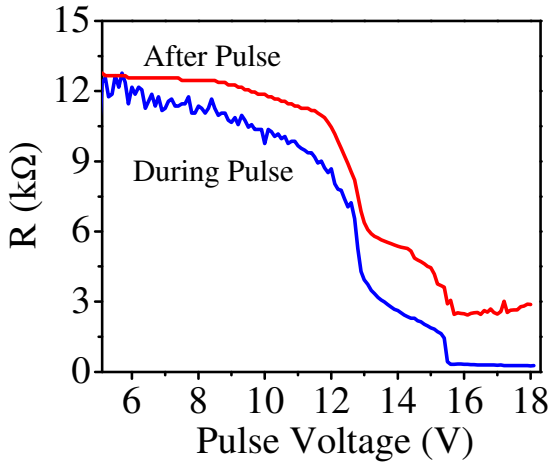


Figure 2.2 Resistance of a Si microwire during and after each pulse in a series of 1 μs rectangular voltage pulses with incrementing amplitude (0.1 V).

Another controllable method of annealing the wires is to introduce a resistor (R_L) between the wire and pulse generator (Figure 2.3). In our experimental setup, the coaxial cable used to monitor the voltage in between the load resistor and Si wire (V_{wire}) introduces parasitic capacitance in parallel with the wire. In the case where $R_{WF} < R_L < R_{W0}$, P_{wire} is sufficient for melting an as-fabricated wire. As the pulse voltage (V_{pulse}) is applied, the capacitor begins charging and the wire is heats until the maximum power transfer condition occurs ($R_W = R_L$) and the wire melts. The capacitor discharges through the highly conductive molten wire (liquid wire resistance ($R_{W\text{-}liquid}$) ranges from ~10 to ~200 Ω). V_{wire} is reduced after the discharge, allowing the wire to cool and solidify. Beyond this point, P_{wire} is not sufficient for melting the wire again with the same bias condition since R_W is significantly reduced due to crystallization of the wire. This is seen in Figure 2.3(c) as a sharp peak followed by a plateau in I-t characteristics. Applying an identical, consecutive pulse does not result in melting [27].

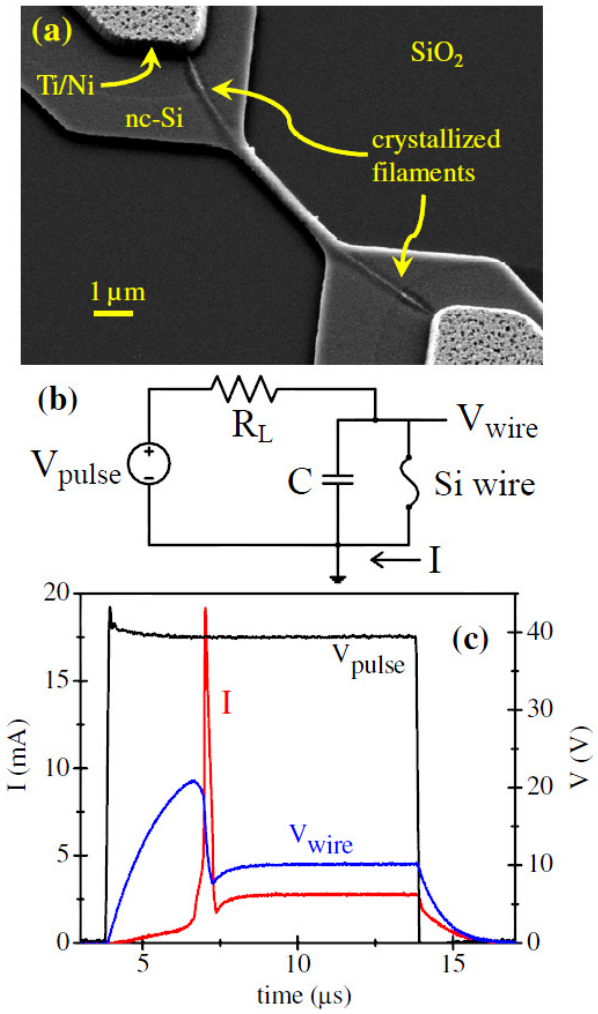


Figure 2.3 (a) SEM of a melted and crystallized Si wire, (b) circuit diagram of the experimental setup, and (c) I-t and V-t characteristics of the wire shown in (a). As fabricated wire resistance = 36.7 kΩ, crystallized wire resistance = 3.7 kΩ, load resistance = 9.9 kΩ.

2.2 Observations of phase change oscillations

Rapid solid-liquid oscillations in the wires are observed while experimenting on crystallization of nanocrystalline Si microwires by pulsing through a load. As stated above, in the case where $R_{WF} < R_L < R_{W0}$, P_{wire} is sufficient for melting an as-fabricated wire but not a crystallized wire. However, in the case where $R_L \approx R_{WF}$, P_{wire} can be sufficient for melting both an as-fabricated wire and a crystallized wire, with the maximum power transfer condition satisfied for a crystallized wire. Due to the discharge mechanism of the capacitor, P_{wire} is not sufficient to keep the wire molten and an instability is achieved, hence solid-liquid phase change oscillations occur [15]. The maximum and minimum resistances during the oscillations suggest that a wire can oscillate between completely solid and completely liquid states (Figure 2.4), or between different liquid-solid ratios long the length of the wire (Figure 2.5). Oscillation amplitude and frequency are determined by R_L, R_W in solid state, V_{pulse}, parallel capacitance (C), and the time scale of melting and resolidification. Similar relaxation oscillation behavior is observed in VO_2 structures due to metal-insulator transitions [28, 29].

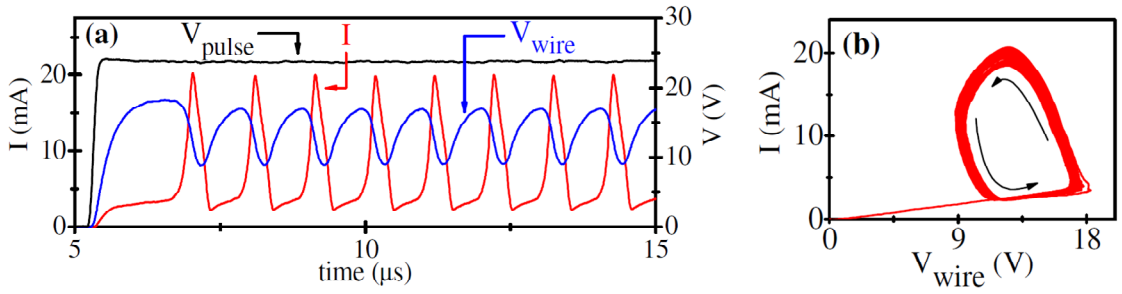


Figure 2.4 (a) I-t, V-t, and (b) I-V characteristics of solid-liquid phase change oscillations in a Si microwire.

Every time a wire melts and resolidifies there is a small change in solid-state wire resistance. Each oscillatory period consists of one cycle of melting and resolidification and oscillation amplitude is slightly different in each period. The system is observed to abruptly lose or gain resonance as R_W solid changes over a typical time scale of ~50 μs in the case presented in Figure 5. In this particular case, R_W increases by approximately three times (to about 50% of R_{W0}) and the system oscillates in four distinct regions. Oscillation frequency is in the order of 1 MHz and it is constant within each region. After ~ 1 thousand cycles of phase-change oscillation the wires typically disconnect due to significant electromigration of Si in liquid state. The Si atoms become ionized due to the substantial thermal carrier generation associated with melting, and do not have restricted movement in the liquid phase, thus the Si atoms drift in the direction of the electric field.

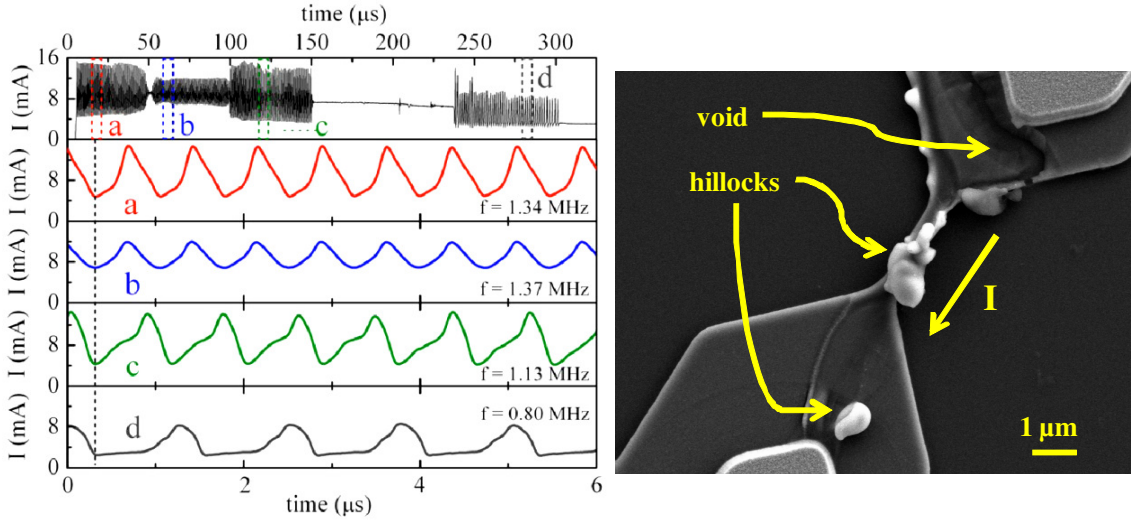


Figure 2.5 I-t characteristics and SEM of a nc-Si microwire which exhibits four distinct regions (a–d), with constant frequencies within each region (1.34, 1.37, 1.13, and 0.80 MHz). R_W before pulse = 2 kΩ, R_{WF} = 5.9 kΩ.

2.3 Pulse generation

In some cases, a wire with a constriction, which may have formed due to previous melting and resolidification of the wire, may disconnect and reconnect repeatedly during phase-change oscillations, resulting in the generation of current pulses [30]. An example of such a wire is shown in Figure 2.6(c), and its I-t characteristics in Figure 2.6(d) show the pulse train between 4 and 8 μs is very stable with consistent pulse shape, pulse width, rise/fall times, repetition rate and amplitude. Figure 2.6(e) shows 30 pulses from the stable region superimposed, aligned by their rising edges. Pulses in the stable region have an average pulse width of 13.48 ± 0.65 ns and repetition rate of 9.12 ± 0.06 MHz. The generated pulses have extremely sharp rising and falling edges which have approximately equal rise and fall times. An average time constant of 383 ± 0.26 ps is extracted from exponential fits to the pulses' falling edges, which is approximately equal to the minimum rise/fall time of the oscilloscope used in the measurements. Thus, the rise/fall times are ≤ 383 ps since the measurements were limited by the oscilloscope used in the measurements. The sharp pulse shape suggests that the pulse train is generated by sudden, repeated electromechanical connection and disconnection of the wire at a constriction (Figure 2.6(c)) formed during the initial crystallization step and the DC I-V measurements. The disconnection is expected to be due to reduction in volume as part of the wire melts, leading to tensile stress which pulls the wire apart at its constriction. Disconnection of the wire prevents the flow of current so the wire is able to cool down and re-solidify. The increase in volume upon solidification results in reconnection of the wire at the constriction and current is able to flow again. The increasing current level during the pulses (~4 to 7 mA) suggests the wire is gradually melting during each

generated current pulse. ~60% of the wire is estimated to be molten at the time of disconnection, based on the resistivity values of the Si film in solid and liquid state (liquid Si resistivity = 75 ± 4.6 μΩ- cm).

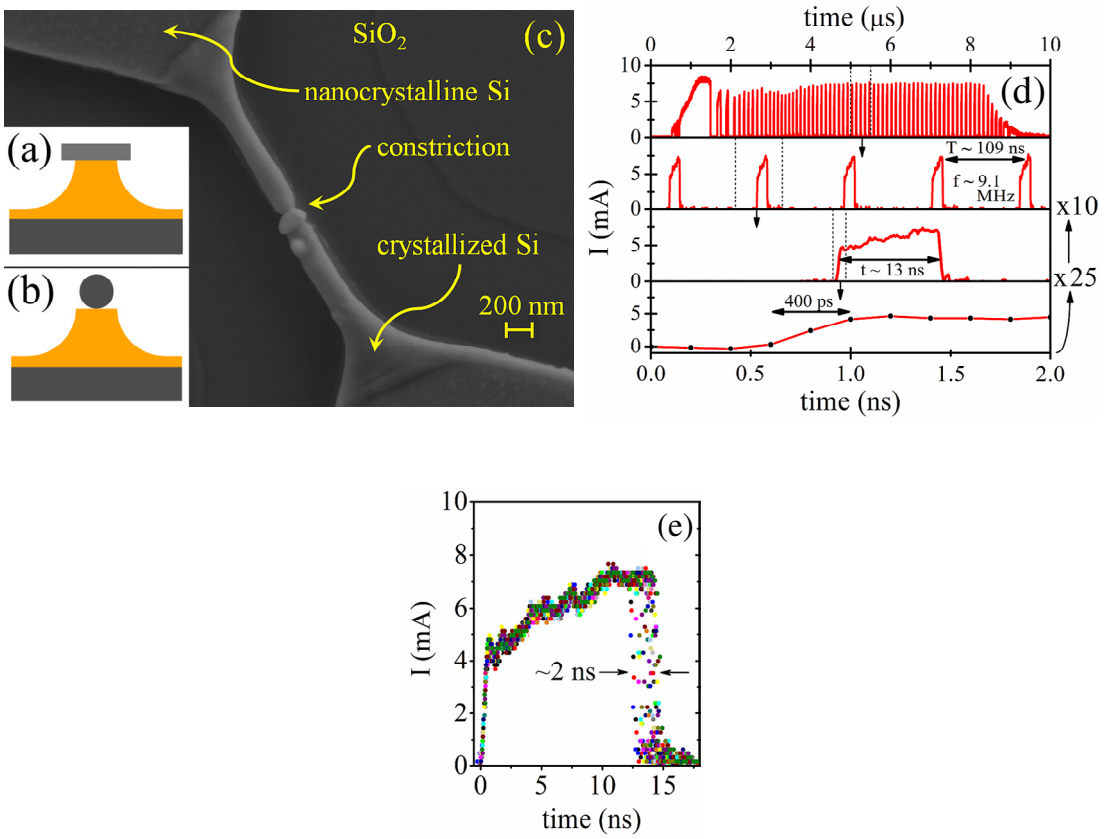


Figure 2.6 Cross-sectional schematics of a partially undercut wire (a) as-fabricated and (b) melted and crystallized. (c) SEM image of a crystallized Si wire with a constriction near the midpoint. (d) I-t characteristics of the Si wire during pulse generation shown in 10 μs, 500 ns, 50 ns and 2 ns timescales. The segment indicated between dotted lines in each pane is expanded in the pane below. One data point is acquired every 200 ps. The wire was biased with a 17.5 V, 8 μs rectangular voltage pulse. (e) 30 current pulses from the stable region (4–8 μs) plotted on top of each other, aligned by their rising edges.

2.4 Device and frequency scaling in SOI structures

We have fabricated much smaller structures on a silicon-on-insulator (SOI) wafer and scaling effects of the phase change oscillations are demonstrated (Figure 2.7). In the larger nanocrystalline wires, typical values from oscillations are V_{pulse} ~ 20 V, V_{wire} ~ 9–17 V, and I ~ 2–20 mA. The scaled down devices are able to achieve phase-change oscillations with much lower power, where values for complete liquid-solid oscillation were observed to be as low as: V_{pulse} = 6 V, V_{wire} ~ 2.2 – 3 V, and I ~ 0.2 – 2.5 mA. These smaller scale c-Si wires (~ 10 times less volume than the nc-Si wires we have previously reported on) can produce relaxation oscillations with approximately three times smaller supply voltage (6 V) with ~ 40 times smaller peak power [14].

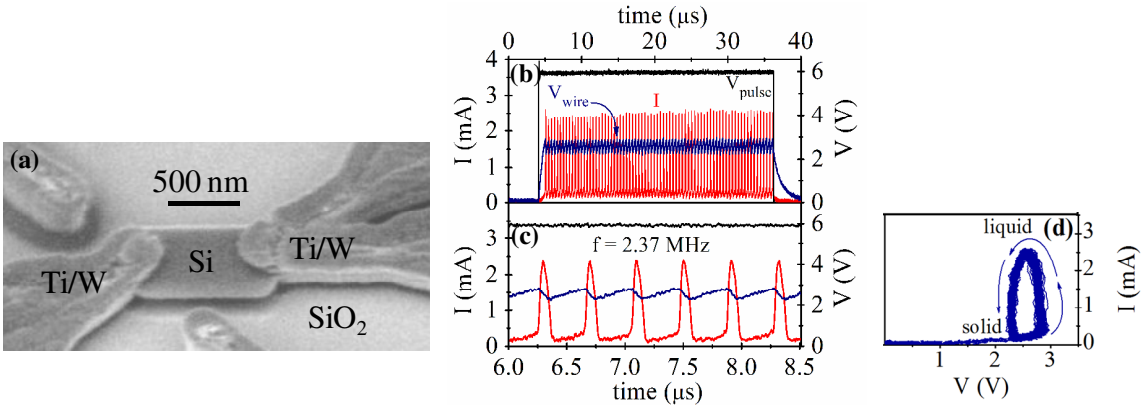


Figure 2.7 (a) SEM image of an as-fabricated single-crystal silicon wire with length ~ 500 nm, after etching with HF to remove passivation oxide for imaging purposes. (b) Experimental I-t, V-t, and (c) I-V characteristics of phase-change oscillations in a crystalline silicon wire.

The effect of scaling capacitance is demonstrated through oscillations produced on the same structure with capacitance values of ~ 30 pF, 31 pF and 40 pF with

corresponding frequencies of 5.53 MHz, 4.80 MHz, and 3.89 MHz (Fig 2.8(a)). Higher frequency oscillations (~ 7 MHz) have been achieved with smaller device length (400 nm) in conjunction with small load capacitance (30 pF). The shields of the coaxial cables used in this experiment were disconnected from ground to minimize parasitic capacitance which leads to ringing between pulses.

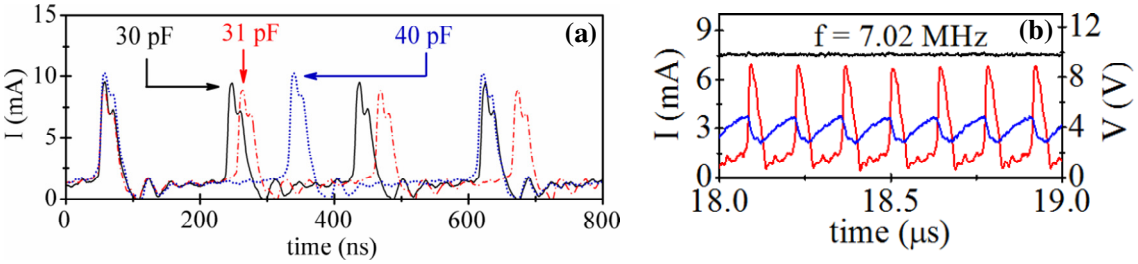


Figure 2.8 (a) Experimental I-t characteristics of phase change oscillations in a c-Si wire with varying values of C and all other parameters kept constant. (b) I-t, V-t, and I-V characteristics of phase-change oscillations with reduced capacitance (C ~ 30 pF).

2.5 Electromigration

An experiment is set up to compare the electromigration observed during the phase-change oscillations to the typical solid-state electromigration that occurs in the solid state. nc-Si n-type wires are stressed with an AC voltage which delivers pulses ~ 2 MA/cm^2 at ~ 8 MHz frequency (Figure 2.9(a)) with enough time in between pulses for the wire to cool to ensure the wires remain in solid state, as suggested by simulation results in Figure 2.9(b). After several hours of the electrical stress the wires exhibit electrical failure due to electromigration of material leading to voids (Figure 2.9(c-e)).

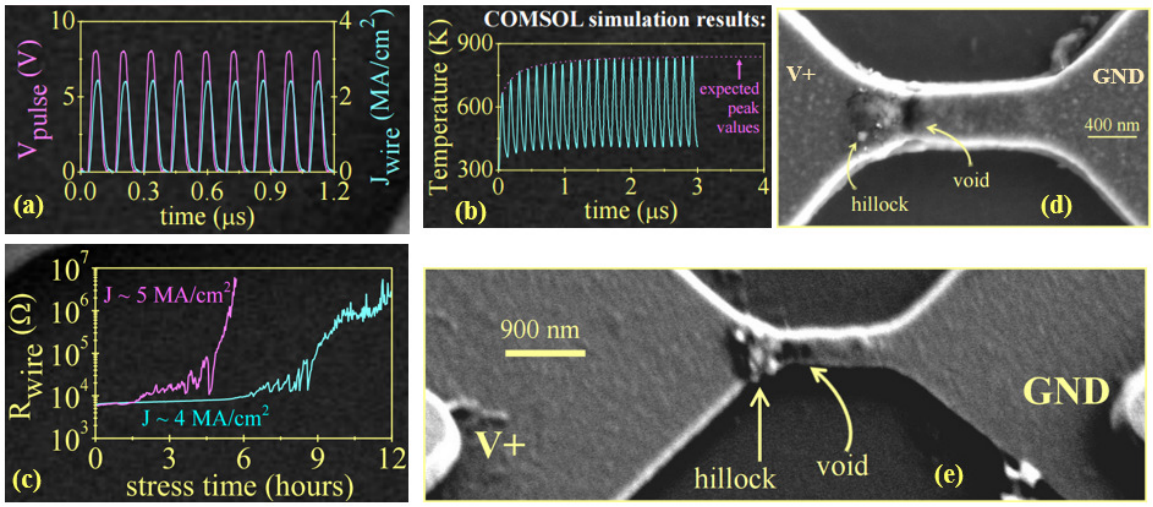


Fig 2.9 (a) Voltage and current vs time characteristics for electrical stress of the wires in solid state. (b) Simulated wire temperature during the electrical stress. (c) Wire resistance vs. time during electrical stress. (d,e) SEM images showing void formation resulting from electromigration [31].

The amount of material that moves is much less than what is observed in the oscillations, although the void formation is still significant. Here, the material is moving in the opposite direction than in the oscillations and the electromigration occurs from the force of high velocity electrons during repeated large current density stress, resulting in the hillocks and voids being in much closer proximity than in the phase change oscillations where the Si atoms are moving with the direction of electric field as the material is ionized in the liquid state.

The main challenge for phase-change oscillators is frequency stability and device reliability due to electromigration of silicon at high temperatures which causes wires that are not encapsulated to change shape, leading to frequency drift or intermittent oscillations and eventual failure. Since the solid–liquid oscillation frequency is

determined by the power dissipated and charging and discharging of the parallel capacitor, it is very sensitive to any volume and shape variation of the Si wire. Thus far experimental work has not been performed on structures that are optimized for phase-change oscillations, and devices experience catastrophic failure after 1 s of operation. The devices could potentially be improved – optimum device geometry and surrounding materials could be investigated to address the frequency stability and device integrity problem. Devices encapsulated in a thick, hard shell of silicon nitride are expected to be less vulnerable to changes in shape and size during the solid–liquid transitions. Additionally, frequently alternating the polarity of voltage could mitigate the migration of material in one direction. If the device reliability can be improved, these phase change oscillator devices are expected to have useful applications in high temperature / high radiation conditions such as nuclear reactors or accident sites where conventional electronics cannot function, as these devices make use of a thermally driven process.

3. Simulation of phase change oscillations

3.1 Simulation setup

COMSOL Multiphysics 3.5 [32] is used to simulate the phase- change oscillations using a finite element, 3-D physical model for the Si wire coupled with a SPICE model for R_L, C, and V_{pulse} to explore the effects of scaling device length, capacitance, load resistance, and supply voltage (Figure 3.1(a)). Temperature dependent electrical resistivity (ρ) and thermal conductivity (κ) for n-doped (10^{19} cm^{-3}) c-Si are used in the simulations (Figure 3.1(b)). The solid-liquid phase change is simulated by incorporating the latent heat of fusion of Si as a ~ 1000 times increase in the heat capacity (C_P) between 1687 K and 1690 K [33] (Figure 3.1(b) inset). The phase change is accompanied by drastic changes in electrical and thermal conductivities in this temperature range. The 5% increase in mass density upon melting is neglected in these simulations [34].

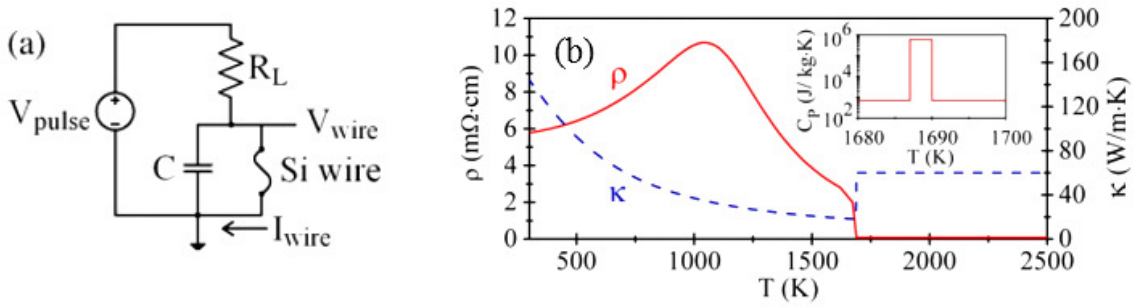


Figure 3.1 (a) SPICE circuit in which the Si wire is represented by the finite element model. (b) Temperature dependent electrical resistivity (ρ), thermal conductivity (κ), and (inset) heat capacity (C_P) for n-type (10^{19} cm^{-3}) single-crystal Si used in the simulations.

The electrical resistivity of c-Si is extracted from Synopsys Sentaurus simulation tools [35] in the 300-1610 K range. The data from 1610 K to melting (1687 K) is obtained from experimental results by Sasaki et al. [24] which include phase transition and the liquid value. The thermal conductivity is extracted from Sentaurus in the 300-1687 K range. Thermal conductivity in liquid state is obtained from experimental results by Ong et al. [36].

COMSOL 3-D finite element simulations of joule heating in the Si wire are performed by coupling Heat Transfer by Conduction and Conductive Media DC [12] physics modules. The heat transfer model includes heat diffusion and joule heating:

$$d \cdot C_P(T) \cdot \frac{dT}{dt} - \nabla \cdot (\kappa(T) \cdot \nabla T) = J \cdot J \cdot \rho(T) = Q \qquad \textit{eq (3.1)}$$

where d is mass density, J is current density and Q is power density. The current continuity model includes only the drift term:

$$-\nabla \cdot (\sigma(T) \cdot \nabla V) = 0 \qquad \textit{eq (3.2)}$$

where σ is electrical conductivity and V is electric potential. Diffusion current is ignored since it is expected to be negligible in this case of highly doped Si. Thermoelectric contributions to (3.1) and (3.2), the electrical breakdown of Si (~ 3 x 10^5 V/cm), velocity saturation and mechanical stress are not accounted for due to the additional complexity. Electrical breakdown is expected to enable higher frequency operation for wire lengths ≤ 100 nm due to field dependence of conductivity, allowing for faster melting. The 3-D model of the wire is inserted into a SPICE simulation as a resistive element along with the DC supply, R_L and C (figure 3(b)). The SPICE model and the 3-D finite element model are solved self-consistently to capture the circuit response to any temperature change in the Si wire and vice-versa.

3.2 Modeling the oscillations in SOI structures

Simulated phase-change oscillations capture the general phenomenon that is taking place and have frequencies in close agreement with experimental results. Figure 3.2 shows results of a simulated device which melts and solidifies periodically at a rate of 8.79 MHz. Scaling effects and frequency control of the phase-change oscillator device are studied by varying one parameter at a time in the simulations (Figure 3.3). Sustained oscillations are achieved if the energy required for phase-change (latent heat) can be delivered from the capacitive discharge and the power dissipated in the wire is insufficient to keep it in molten state after discharge, limiting the range of scaling for any subset of parameters. Limits of scaling for each variable are indicated with vertical dotted lines in Figure 3.3 for the subset of parameters shown in Table 3.1. In the length-scaling case the vertical line represents the length at which electrical breakdown becomes significant. The scaling dependencies of oscillation frequency are extracted as:

$$\frac{df}{dV_{pulse}} = 9\frac{MHz}{V}, \quad \frac{df}{dR_L} = -22\frac{MHz}{k\Omega}, \quad \frac{d\log f}{dL} = -0.84\frac{\log(MHz)}{\mu m}, \quad \frac{d\log f}{d\log C} = -0.86\frac{\log(MHz)}{\log(pF)}$$

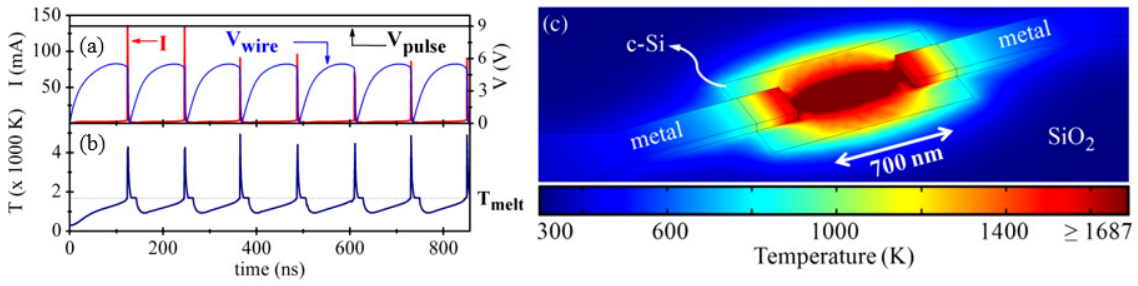


Figure 3.2 (a) I-t, V-t, and (b) T-t characteristics of a simulated phase-change oscillator device computed by COMSOL Multiphysics software. A horizontal dotted line denotes the melting temperature of Si. (c) Three-dimensional finite-element model of a c-Si wire during melting.

Scaled Parameter	V_{pulse} (V)	R_L (kΩ)	L (nm)	C (pF)
V_{pulse}	varied	1	700	20
R_L	9	varied	700	30
L	9	1	varied	20
C	9	1	700	varied

Table 3.1 Parameters used to simulate the scaling effects in Figure 3.3. For all simulations, 700 nm width and 55-nm thickness are used for wire dimensions.

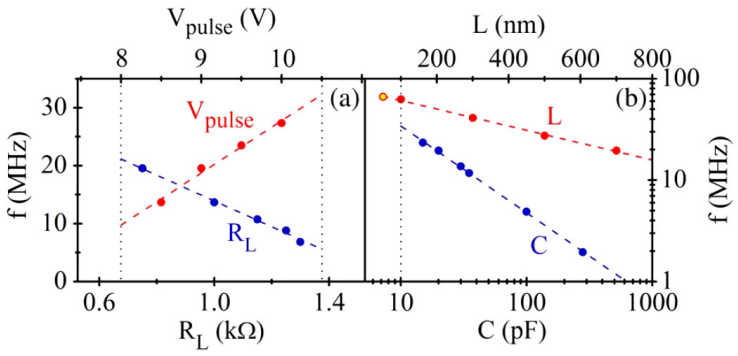


Figure 3.3 (a) Oscillation frequency vs. load resistance, supply voltage, (b) wire length, and capacitance. In each case, all parameters are kept constant except for the one which is being varied. Vertical dotted lines mark the limits of scaling for a single parameter for the given subset of parameters shown in Table 3.1.

3.2 GHz oscillations at the nanoscale

The scalability and frequency limitations of the phase change oscillator device concept are studied by finite element simulations of smaller wires with smaller capacitance than those used in the experiments. Wire sizes are relatively large (1 μm and 100s of nm dimensions) in the experiments and the oscillation frequency is limited by the

parasitic capacitance which cannot be reduced beyond 10 pF with the current setup. High frequency (GHz) oscillations require significantly smaller devices and reduced parallel capacitance. In this section, the physical limitations of this device concept are explored through modeling the device scaled down to nanowire size with parallel capacitance on the order of 10s of fF (Figure 3.4).

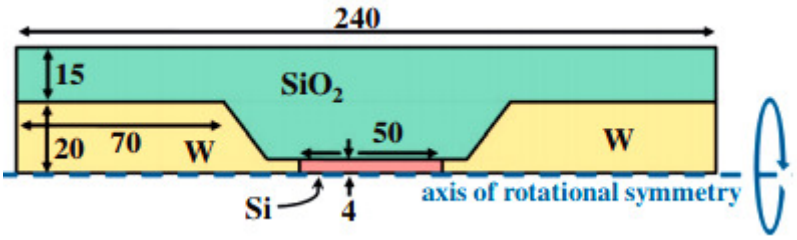


Figure 3.4 A 2-D axial-symmetric finite element model of the silicon nanowire with dimensions marked in nm.

The same modeling techniques from the previous section are employed, however an additional field-dependent electrical conductivity term σ' (Figure 3.5) is added to the temperature dependent conductivity to model electrical breakdown at high electric fields [37].

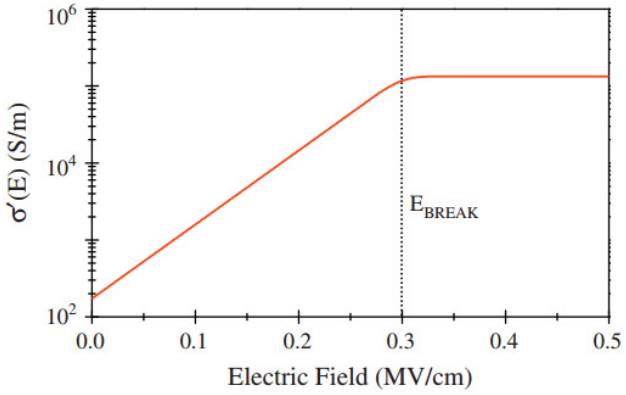


Figure 3.5 An electric field-dependent term for conductivity which is added to σ(T) to model electrical breakdown.

The simulated phase change oscillations capture the phenomenon of repeated melting and freezing of the Si wire as a result of repeated charging and discharging of the parallel capacitor. There is reasonable agreement in the waveform shapes between experimental and simulated data (Figures 3.6 and 2.4), also suggesting that the model captures the general phenomenon of phase-change oscillations.

Scaling capacitance for potentially higher frequencies, as well as tunability of this oscillator, is explored through a series of simulations in which C is varied from 30 to 55 fF and the other parameters are kept constant (V_{DC} = 4.2 V, R_L =7 kΩ). Results show that oscillation frequency has a strong dependence on capacitance, as frequency is determined by the RC time constant associated with charging/discharging. Figure 3.7 shows temperature–time and current–time characteristics of simulated, sustained phase change oscillations for various capacitance values, where the effects of capacitance can be clearly observed. The silicon nanowire reaches higher maximum temperatures and lower minimum temperatures during oscillation for higher capacitance values since a larger capacitor stores and discharges a greater amount of charge. Heating and cooling between

a greater range of temperatures requires more time per oscillation period, also contributing to decreased frequency for higher capacitance. Figure 3.9(a) shows minimum and maximum temperature during oscillations as well as frequency as functions of capacitance, extracted from Figure 3.7.

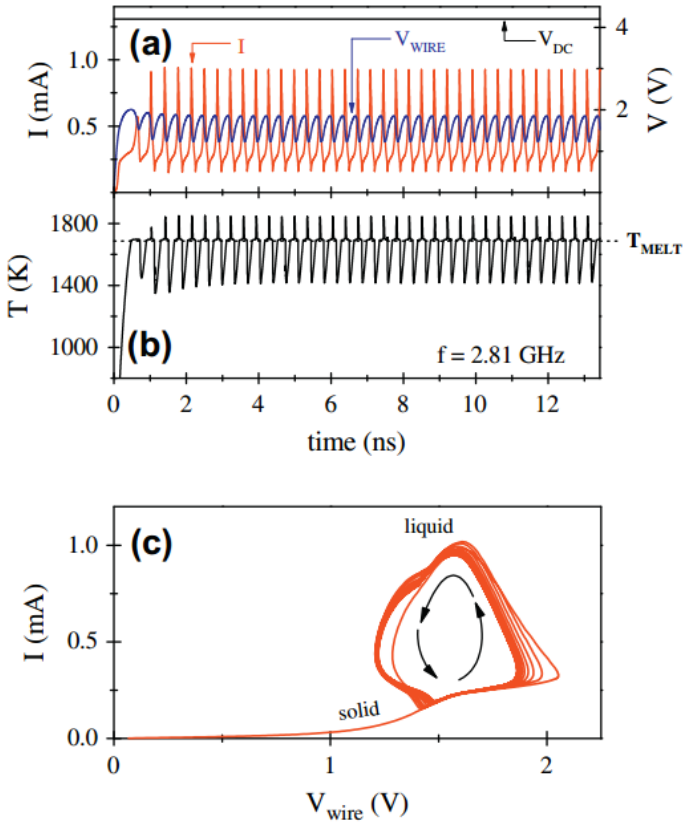


Figure 3.6 (a) Current–time, voltage–time characteristics, (b) temperature–time characteristics, and (c) current–voltage characteristics during simulated phase change oscillations with V_{DC} = 4.2 V, R_L = 7kΩ, C = 40 fF, wire length = 50 nm, wire diameter = 8 nm. Frequency = 2.81 GHz, extracted for t > 3 ns, where the oscillations have stabilized.

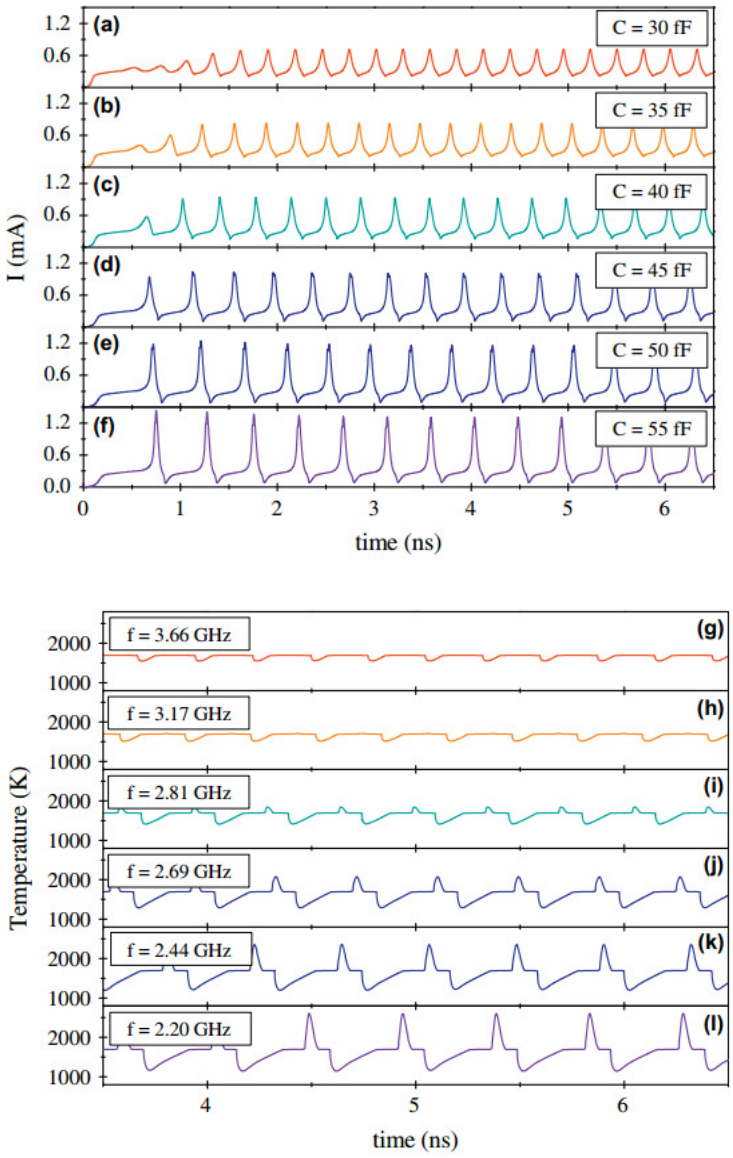


Figure 3.7 Current–time and temperature–time characteristics during simulated, sustained phase change oscillations in a Si wire for various capacitances: (a and g) C = 30 fF, (b and h) 35 fF, (c and i) 40 fF, (d and j) 45 fF, (e and k) 50 fF, (f and l) 55 fF. Corresponding frequencies are 3.66 GHz, 3.17 GHz, 2.81 GHz, 2.69 GHz, 2.44 GHz, and 2.20 GHz, respectively. V_{DC} = 4.2 V, R_L =7kΩ, wire length = 50 nm, wire diameter = 8 nm.

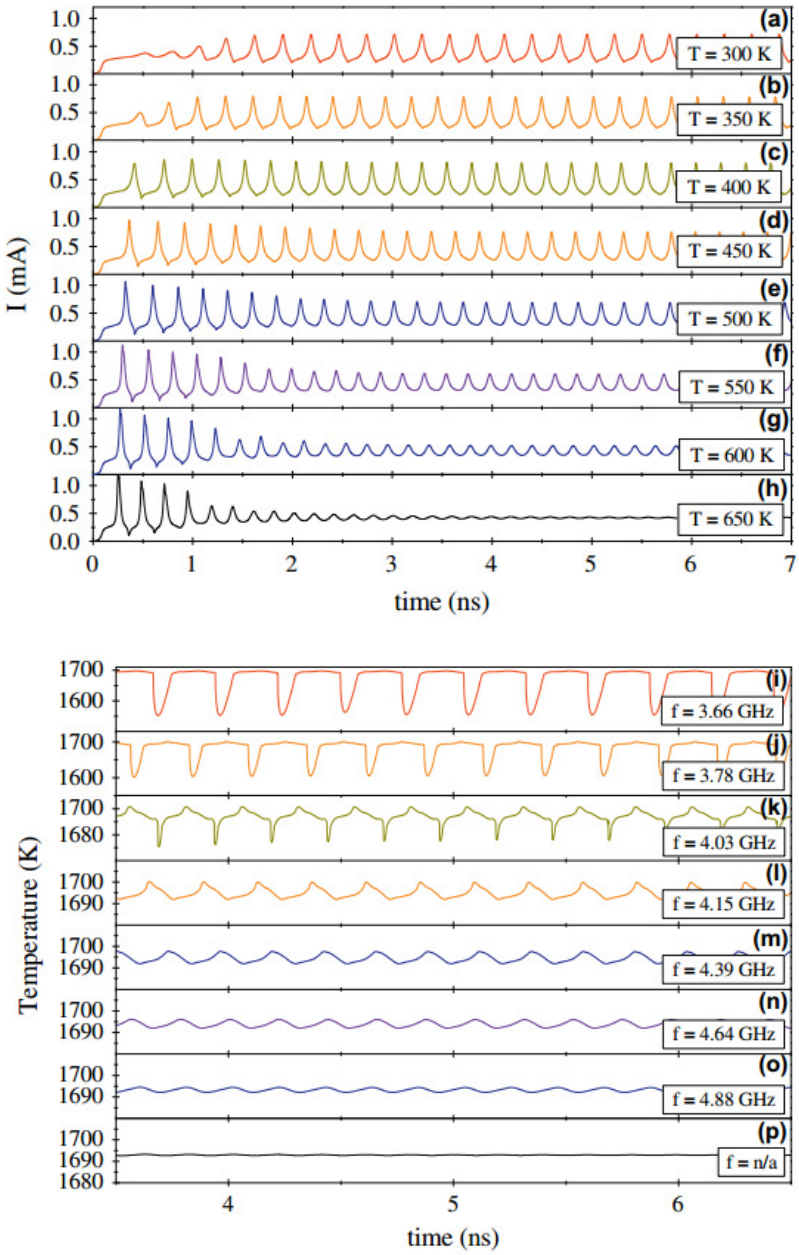


Figure 3.8 Current–time and temperature–time characteristics during simulated phase change oscillations at various ambient temperatures: (a and i) T = 300 K, (b and j) 350 K, (c and k) 400 K, (d and l) 450 K, (e and m) 500 K, (f and n) 550 K, (g and o) 600 K, (h and p) 650 K. Corresponding frequencies are 3.66 GHz, 3.78 GHz, 4.03 GHz, 4.15 GHz, 4.39 GHz, 4.64 GHz, 4.88 GHz, and (h) does not have sustained oscillations. V_{DC} = 4.2 V, R_L =7kΩ, C = 30 fF, wire length = 50 nm, wire diameter = 8 nm.

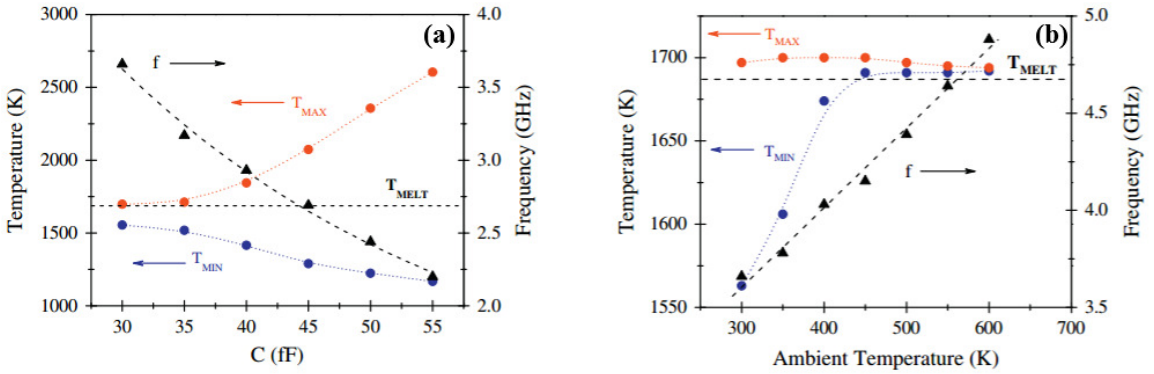


Figure 3.9 (a) Minimum and maximum temperature in the core of the Si wire during sustained phase change oscillations, and frequency, as functions of capacitance, extracted from Figure 3.7. (b) Minimum and maximum temperature in the core of the Si wire during sustained phase change oscillations, and frequency, as functions of ambient temperature, extracted from Figure 3.8.

In the case of Figure 3.7(c, i) (V_{DC} = 4.2 V, R_L =7kΩ, C = 40 fF), the average power dissipated in the Si wire is 588 μW, while the average power delivered to the 7 kΩ load is 975 μW. Our model predicts this oscillator device concept to have 2-3 orders of magnitude higher power density than a conventional CMOS oscillator [8-13], as the simple circuit with a Si nanowire, 40 fF capacitor and poly-Si resistor can be fabricated in an area < 6 μm^2.

The phase-change oscillators are expected to be compatible with high temperatures since the resistance switching property (solid–liquid transition) occurs at a very high temperature (1687 K). However, as the oscillator frequency depends strongly on thermal losses to the surroundings, the frequency and amplitude of oscillations are expected to change significantly depending on the ambient temperature. Another series of simulations is performed in which the ambient temperature is varied from 300 K up to 700 K with all other parameters constant (V_{DC} = 4.2 V, R_L =7kΩ, C = 30 fF). At elevated

temperatures, less electrical energy is needed to bring the wire into molten state, and heat in the nanowire does not diffuse out as fast. Fig. 3.8 shows current–time and temperature–time characteristics of simulated phase change oscillations at elevated ambient temperatures. Devices in higher temperature environments reach a higher maximum temperature earlier, however once the oscillations have stabilized the temperature oscillates more closely about the melting temperature since the wire does not cool as quickly and thus retains more heat. Once ambient temperature becomes sufficiently large (for a chosen set of parameters which force oscillations at room temperature) then the energy from the bias condition in conjunction with the elevated ambient temperature is sufficient for keeping the wire in liquid state and hence no phase change oscillations can be achieved. Figure 3.9(b) shows that the core temperature of the Si wire does not drop below the melting temperature during oscillations, a result of the wire oscillating between completely liquid and partially liquid states. However, since the frequency is directly tunable by the DC bias applied, load resistance and parallel capacitance, a temperature compensating circuit can be integrated with the device to adjust the voltage, load resistance or capacitance depending on the sensed temperature. This is similar to what is currently done for crystals, MEMS and CMOS based oscillators for temperature compensation to achieve frequency stability over the typically required temperature range of -40 C to +85 C. Being fully compatible and monolithically integrated with the CMOS circuitry this temperature compensation is expected to be easy to achieve for phase change oscillators [38].

4. Simulation of electrical device operation of phase change memory

4.1 Simulation Setup

Two-dimensional finite element simulations of reset operation in PCM cells are performed using COMSOL Multiphysics software [32] to predict how variations in geometry and load resistance affect device performance [39]. In particular, we examine the confined cell [40], similar to the well-known mushroom cell design [17] except that the phase change material is extended into the confined pillar (Figure 4.1). In our simulations we incrementally recess the bottom contact, extending the active region into the confined heater and compare a range of confined cell geometries. The structures are typically meshed with ~5000 points with increased mesh density in the active region. Temperature dependent electrical and thermal conductivities (σ and κ, respectively) for GST are taken from experimental results [41-43] as shown in Figure 4.2(a). The latent heat of fusion (L_f = 126 x 10^3 J/kg [44]) is incorporated as a spike in heat capacity (C_P) [33] at the melting temperature [45], as illustrated in the inset of Figure 4.2(a). Mass density (d) of GST is modeled as a constant at 6200 kg/m^3 [46] and contributions due to stress and strain are not included in this study. Temperature dependent σ and κ are also used for TiN, as shown in Figure 4.2(b). C_P and mass density of TiN are modeled as constants of 784 J/kg·K [47] and 5430 kg/m^3 [48], respectively. The and heat transport equation and current continuity equation, as previously given in *eq (3.1)* and *eq (3.2)* respectively, are solved self-consistently using COMSOL Multiphysics, assuming charge neutrality.

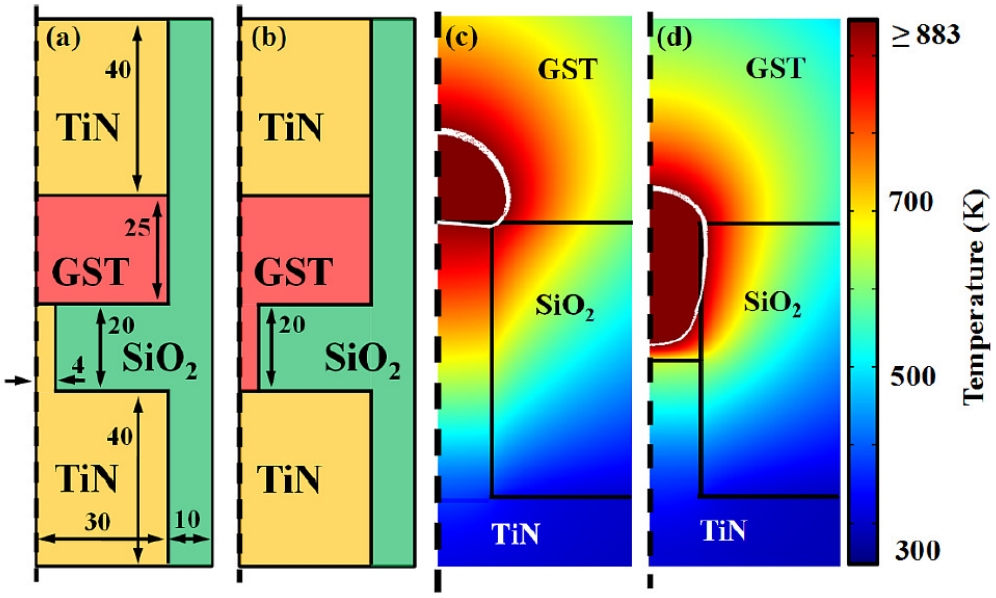


Figure 4.1. (a) Schematics of a conventional planar mushroom cell design with an extension of the $Ge_2Sb_2Te_5$ (GST) active region with dimensions marked in nm, and (b) a confined cell with 20 nm GST extension length. (c) Peak thermal profile of a planar mushroom cell with 25 nm film thickness during reset pulse (biased with 0.83 V) compared to (d) a confined cell with 25 nm film thickness and 10 nm GST extension length (biased with 0.76 V). Dotted lines mark the axis of rotational symmetry in each case, and a white contour line denotes the boundaries of melting in the active region.

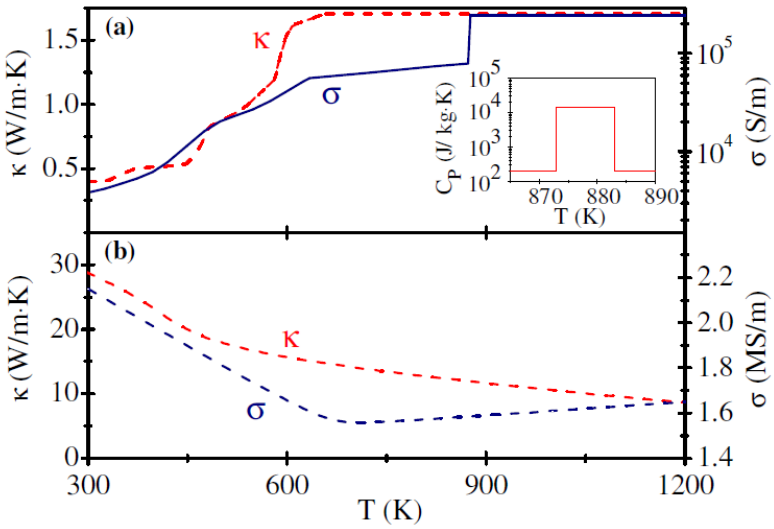


Figure 4.2 (a) Temperature dependent thermal and electrical conductivity for crystalline (FCC) GST, and (inset) heat capacity incorporating the latent heat of fusion. (b) Temperature dependent thermal and electrical conductivities of TiN.

Unlike many earlier studies in the literature [49-51], temperature dependent material parameters [37] are used to more accurately simulate device performance. Joule heating in materials with a negative temperature coefficient of resistivity (such as phase change materials) is a process with positive feedback since an increase in current flow causes an increase in temperature, and vice versa, and simulations with only constant-value parameters cannot capture this non-linear behavior of the heating. Figure 4.3 shows a comparison between simulations with our temperature dependent model and with constant-value parameters [49-51], where the same volume of GST is melted for each case for the comparison. The simulations with the constant-value model show constant current throughout the duration of the pulse, and voltage is being significantly overestimated while the current is underestimated. The non-linear heating effects cannot

be captured with a model with constant-value material parameters and it is important to use a temperature dependent model to accurately predict device performance.

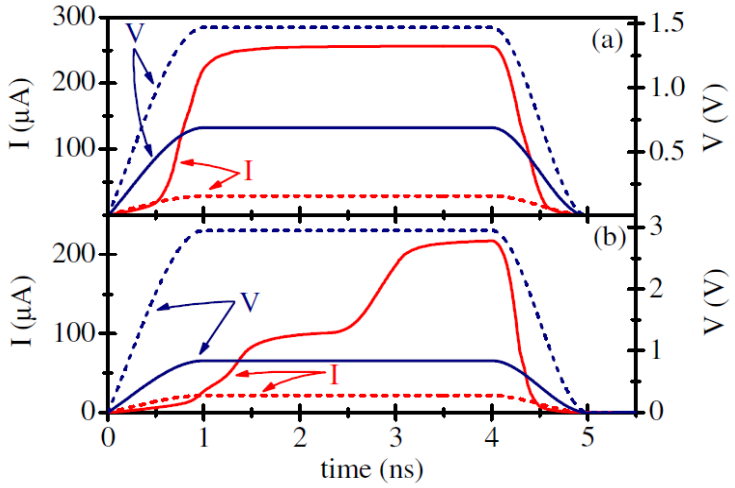


Figure 4.3 I-t and V-t characteristics of reset operation comparing constant value parameters to temperature dependent parameters for reset operation of cells with a 1 kΩ load, 15 nm GST film thickness and (a) 4 nm GST extension length and (b) 16 nm extension length. The same volume of GST is melted for the comparison between the constant-value model [49-51] (dotted lines) and temperature dependent model (solid line).

4.2 Device geometry variations

Simulation results indicate that a significant reduction in maximum reset current can be achieved by extending the GST active region into the confined pillar (Figure 4.4). As illustrated in Figure 4.1(c, d), an extension of the GST active region results in a more favorable thermal profile for heating the entire width of the confined pillar (pillar diameter = 8 nm). The reset current is minimized at ~ 210 μA for a GST extension length between 8 and 16 nm, and this is approximately two times reduction in both reset current

and power compared to the conventional planar mushroom cell. However, reset current does not continue to reduce significantly beyond an extension length of 10 nm while the power consumption continues to increase (Figure 4.4(c)), since an excessive amount of GST is being melted in devices with longer extension lengths. Thus, a device with a GST extension length of ~ 8–10 nm predicted to have optimum performance. This extension length is comparable to the heater diameter for the most favorable thermal profile (Figure 4.1(d)).

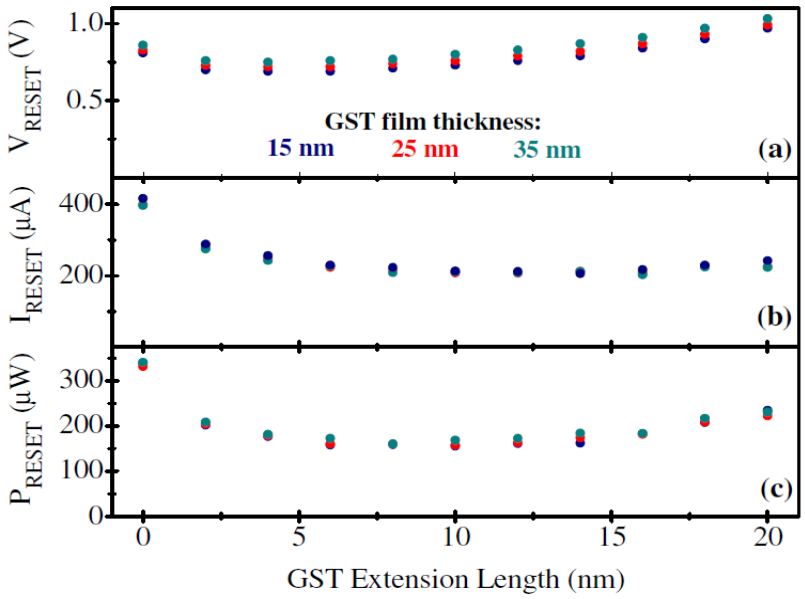


Figure 4.4 (a) Pulse voltage, (b) peak current and (c) peak power during reset as a function of the GST active region extension length.

Figure 4.5 shows current–time characteristics during reset operation for all PCM cells in the simulations. The planar mushroom cells and pore cells with a short extension length (10 nm) show non-linear transitions in current throughout the duration of the pulse, where the active region does not melt until t > 2 ns. However, we find that this instability

in current, which is also seen experimentally [52], is not a result of cell geometry but rather it is related to the load resistance conditions. In this set of simulations, the GST extension length and thus overall cell resistance is increasing while the load resistor remains constant at 1 kΩ for each case. The planar mushroom cell, with 15 nm GST film thickness and its active region in a liquid state during the reset pulse, has resistance ($R_{Cell-Lq}$) ~1 kΩ and matches the load; thus the maximum power transfer condition is reached. Further melting leads to reduced power in the cell, hence stability is achieved between positive-feedback and negative-feedback conditions. The pore cell with 15 nm GST film thickness and 20 nm extension length has $R_{Cell-Lq}$ ~3.4 kΩ, significantly greater than the 1 kΩ load, so the maximum power transfer condition is not reached and hence stability is not achieved.

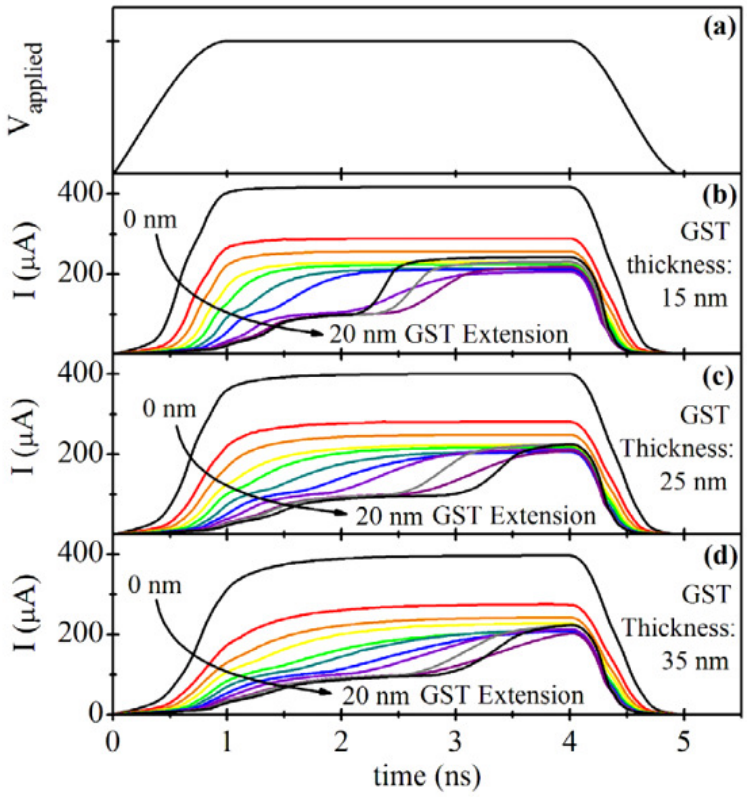


Figure 4.5 (a) Voltage–time and (b)–(d) current–time characteristics during reset operation for all cell geometries.

Our simulation results predict improved PCM cell performance by moderately extending the active region of GST into the heater with a recess comparable to the heater diameter (Figure 4.4). The reset currents and power consumption are reduced by about two times compared to a conventional planar mushroom cell of the same size, due to heat confinement. Also, we have demonstrated that simulations which use constant values for material properties are substantially underestimating the current and overestimating the voltage and cannot capture the non-linear behavior of the Joule heating which is also observed in the experimental studies [52].

4.3 Load resistance effect

Our simulations with the temperature dependent model indicate that load resistance in series with the PCM cell has a significant effect on the current-time characteristics. When the load resistance (R_L) is much smaller than $R_{Cell\text{-}Lq}$, there is nothing to limit the thermal runaway. When $R_L \approx R_{Cell\text{-}Lq}$ the cell voltage decreases as it heats, resulting in a self-limiting and more stable heating process. A series of simulations is performed where cells are biased with a range of voltages for three cases of load resistance ($R_L < R_{Cell\text{-}Lq}$, $R_L = R_{Cell\text{-}Lq}$, $R_L > R_{Cell\text{-}Lq}$) – with the minimum voltage being insufficient for melting any GST, and the maximum voltage being sufficient for a full reset condition in which all GST across the confinement is melted. The results are shown for a confined cell with 20 nm extension length in Figure 4.6. When $R_L < R_{Cell\text{-}Lq}$, only a very small difference in supply voltage (20-40 mV) separates a full-reset operation from not melting any GST whatsoever, indicating a very clear voltage threshold. When $R_L \geq R_{Cell\_Lq}$, a much larger voltage difference (> 140 mV) separates a full reset operation from not melting any GST. The intermediate plateau in the current is limited to the transient time. In the $R_L > R_{Cell-Lq}$ case, the strong negative feedback induced by further melting is expected to result in better stability for higher amplitude and longer duration pulses. Hence, the PCM cells and electrical operation conditions have to be designed with the consideration of the $R_L = R_{Cell-Lq}$ condition, the desired resistivity contrast and power consumption.

While latent heat of fusion upon melting is expected to lead to added stability, increased electrical conductivity leads to positive feedback and thermal runaway

depending on the load conditions. This is also seen as a distinct threshold voltage between non-molten and fully reset conditions for low load resistance values.

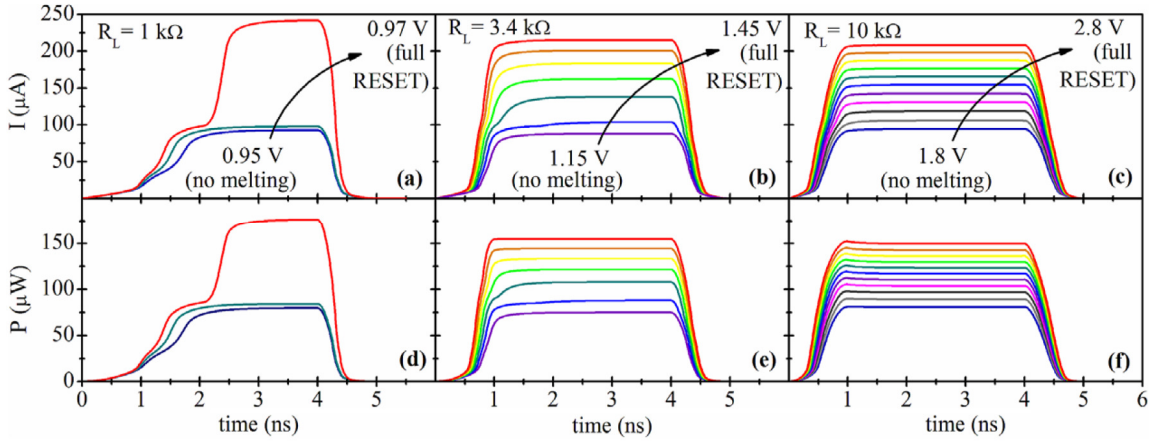


Figure 4.6. (a-c) Current-time and (d-f) power-time characteristics for a confined cell with 20 nm GST extension length and 15 nm GST film thickness, for a range of supply voltages: from a voltage insufficient for melting any GST to a voltage sufficient for a full reset operation. Cell resistance with liquid active region is ~ 3.4 kΩ. Maximum power transfer condition is not reached in (a,d), is achieved in (b,e), and is crossed through in (c,f).

Our simulation results predict improved PCM cell performance by moderately extending the active region of GST into the heater with a recess comparable to the heater diameter. The reset currents and power consumption are reduced by ~ 2 times compared to a conventional planar mushroom cell of the same size due to heat confinement. Temperature dependent electrical and thermal conductivities as well as the latent heat of fusion for GST are incorporated for a significantly improved model of device operation during a reset pulse, demonstrating the possibility of positive-feedback and thermal runaway depending on the load conditions. Also, we have demonstrated that simulations

which use constant values for material properties are substantially underestimating the current and overestimating the voltage and cannot capture the non-linear behavior of the Joule heating which are also observed in the experimental studies [52].

5. Modeling Crystallization in $Ge_2Sb_2Te_5$

5.1 Modeling Approaches

In the previous section, a finite element model for simulating reset operation of a PCM cell that captures the crystalline to liquid phase change is demonstrated. This model is built upon to also capture the amorphous to crystalline phase change as well as the liquid to amorphous phase change, allowing for simulating set operation as well as cycling a device. Modeling the amorphous to crystalline phase change can be achieved by simulating the nucleation and growth of crystal grains within an amorphous matrix. Nucleation and growth rates in the GST at each mesh point and each timestep in the simulation can be calculated based on the temperature profile in the material using the literature data for temperature dependent nucleation and growth rates [22]. Nucleation is most significant at lower temperatures (~ 500 K) and diminishes at higher temperatures where growth is most significant (~870 K) for GST (Figure 5.1). Crystal nuclei are generated via a probability function based on the nucleation rate, mesh size and timestep in the simulation, and expand into crystal grains according to the growth rate. Amorphization of crystalline material is also modeled by resetting the phase to amorphous for any GST that has exceeded the melting temperature. This modeling approach can be used to predict the crystallization of an arbitrary GST structure during any annealing such as joule heating or laser annealing, suggesting where crystallization begins from and the distribution of grain sizes. A crystallinity variable '***c***' can be assigned to each point in the GST, where a value of zero or one represents amorphous or crystalline material, respectively, allowing for dynamic updates of the material parameters during the simulation. Using a crystallinity variable to represent the

dynamically changing grain shapes and material properties within one heavily meshed domain is a more efficient and simpler technique than generating separate individually meshed domains for the grains (Figure 5.2(a)).

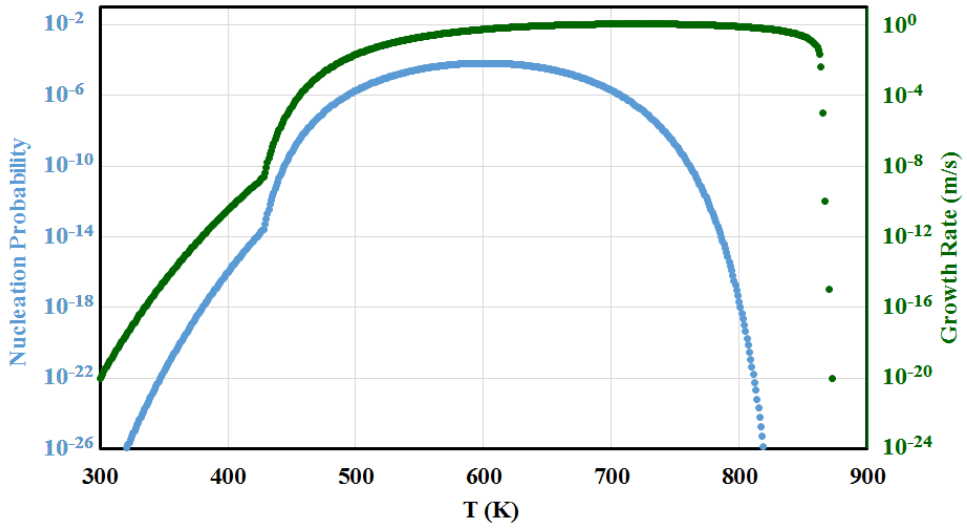


Figure 5.1 Nucleation probabilitiy and growth rate as functions of temperature. Data is taken from [22]. Nucleation probability is calculated from nucleation rate and mesh size and time step, 10 nm^3 and 5 ns in this case, respectively.

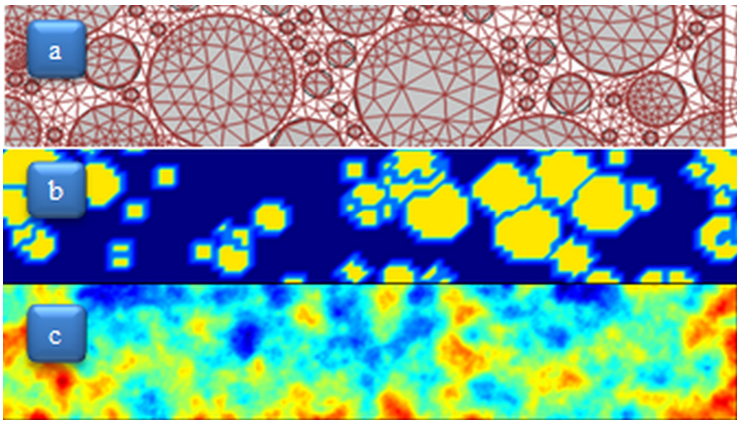


Figure 5.2 (a) Domain based model with individually meshed domains. (b) Mesh based model with binary switch. (c) Effective media model representing the local crystal density in an area.

Two methods of handling the logistics for crystal nucleation and growth for this model are examined – the first method calls an external MATLAB function to assign the values for the crystallinity variable $\boldsymbol{c}$, and the second method utilizes a rate equation for $\boldsymbol{c}$ within COMSOL. Both methods are implementations of a mesh based model as shown in Figure 5.2(b). In the first method, the MATLAB function for the dynamic crystallization model (DCM) takes inputs of the spatial coordinates in the COMSOL model, the timestep and the temperature, and it outputs the crystallinity variable at each point and timestep:

$$\mathbf{DCM(x,\ y,\ z,\ t,\ T)\ =\ } \boldsymbol{c}\big|_{\mathbf{x,y,z,t}}$$

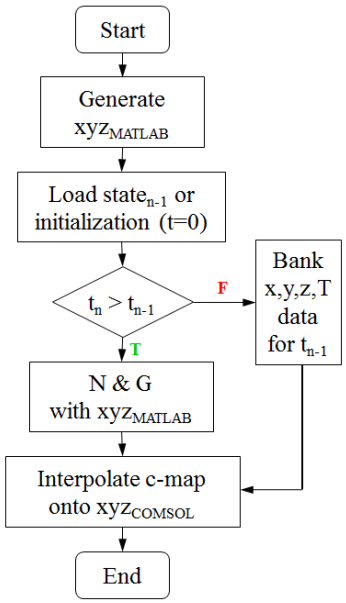


Figure 5.3 MATLAB function and block diagram flow for determining nucleation and growth in the GST.

In the MATLAB method, the details of each grain (size, location and time of nucleation) are kept track of, resulting in a detailed grain map for each simulation. The code for the 2-D function DCM(x,y,t,T) is shown in Appendix 8.2 and the block diagram illustration of the algorithm is shown in Figure 5.3. The DCM function is called at each timestep or intermediate timestep of COMSOL's iterative solver. The regularly spaced grid used in the MATLAB algorithm is intended to match with an identical regularly spaced mesh in COMSOL, however COMSOL generates its own intermediate mesh points during its iterative solving method, hence the need for an interpolation function of the crystal grain map (Figure 5.4). Additionally, COMSOL's iterative solver only computes small sections of the geometry for each of many iterations of a single timestep. As a result, the solutions for each small section of the geometry must be stored (referred to as the Bank in Figure 5.3) until the entire geometry is solved for each distinct timestep. Ultimately, the usefulness of this MATLAB-COMSOL approach has significant limitations stemming from the complexity of the nature of COMSOL's iterative solver and large file I/O times between the two software applications. Various results of GST nanostructure crystallization obtained using this method are shown in Appendix 8.3, highlighting the effect of the laser scan rate on the directionality of the crystallization.

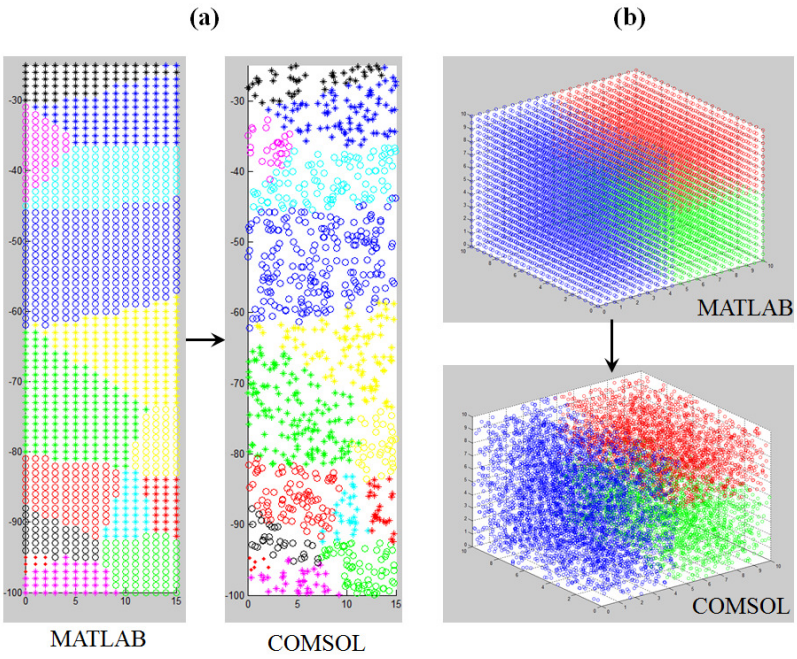


Figure 5.4 (a) 2-D and (b) 3-D crystal grain maps interpolated from a regularly spaced grid in MATLAB onto an irregularly spaced mesh in COMSOL.

The second method for modeling the nucleation and growth by use of a rate equation is developed in collaboration with a fellow group member Zachary Woods, building upon his existing framework which is similar to a phase field model [53, 54]. Zachary developed a crystallization model using a rate equation to track the local crystal density with an effective media approach as shown in Figure 5.2(c). In this effective media model, nucleation and growth of discrete grains are not modeled, but rather the temperature dependent nucleation and growth rates are used to calculate the expected crystalline fraction within local areas. Simulation results using this method are shown in Figure 5.5.

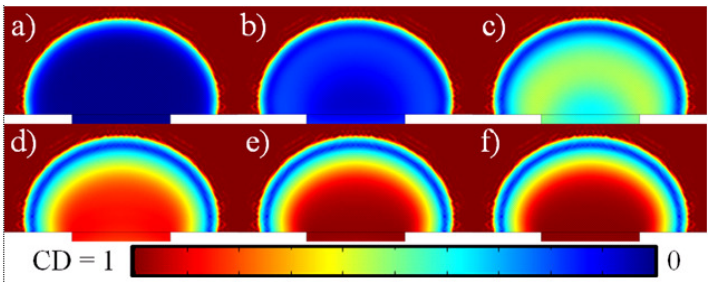


Figure 5.5 Crystal density of a PCM cell during set operation by a low-amplitude, long-duration voltage pulse (50 ns/frame). $R_{initial}$ / R_{final} = 1 MΩ / 6 kΩ. (*Figure credit to Zachary Woods.)*

The terms in the rate equation for the effective media model are altered such that nucleation and growth of discrete grains can be captured, achieving the mesh-based model with binary switch. The rate equation for crystallinity variable $\boldsymbol{c}$ is given by:

eq (5.1)

$$\underbrace{\frac{dc}{dt}}_{\text{crystallization rate}} = \underbrace{f_{nuc}(c,T,rand)}_{\text{evaluates nucleation probability, generates nuclei}} + \underbrace{\nabla\left[f_{growth}(c,T)\cdot\nabla c\right]}_{\text{distributes } c=1 \text{ to adjacent points where } c<1\text{, at a rate based on T}} + \underbrace{f_{amorph}(c,T)}_{\text{forces } c=0 \text{ upon melting}} + \underbrace{f_{stability}(c,T)}_{\text{maintains } 0<c<1}$$

where t is time and T is temperature. In the nucleation term of the rate equation, a random number between 0 and 1 is generated at each mesh point for every timestep and is compared to the nucleation probability at that mesh point, where the nucleation probability is equal to the nucleation rate [$nm^{-3}s^{-1}$] times the mesh size [nm^3] times the timestep [s], just as is done in the MATLAB method. The growth term grows the nucleated grains at a rate equal to the temperature dependent growth rate (Figure 5.1). The amorphization term forces $\boldsymbol{c}$ to 0 for temperatures above the melting temperature (T_{melt} = 873 K). The stability term is used to ensure that the value of $\boldsymbol{c}$ does not increase

to greater than 1 or less than 0, as the model is using a binary representation of amorphous and crystalline areas for c = 0 or 1, respectively. The stability term is essentially a snap-function – the term becomes very large if c is less than zero or becomes largely negative if c is greater than 1, "snapping" the values to either 0 or 1. Likewise, values that are in between 0 and 1 are snapped toward the closer value. Grain boundaries can be distinguished by tracking the locations which have a high dc/dt rate where there is also a high dc/dx. This rate equation method offers the advantage of fast simulation times and the ease of finding convergent solutions compared to the MATLAB approach.

Figures 5.6 – 5.8 show a comparison of simulation results between our COMSOL model and Geoffrey Burr's crystallization model in the literature [22] in which our nucleation and growth rates are taken from. The temperature-time conditions used in our simulations are the same as the conditions from [22]. There is good agreement between the two models despite the vast difference in the computational approaches, as Burr's model is using a sophisticated cellular automata approach that calculates surface energy density and bulk free energy difference between the crystal grains and surrounding amorphous area.

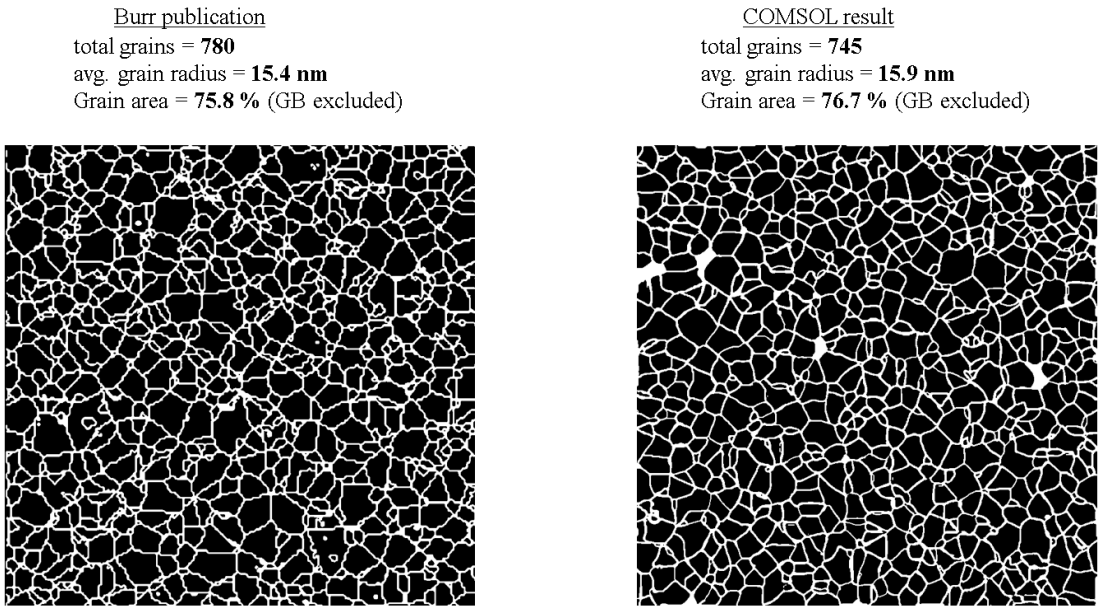


Figure 5.6 Model comparison for crystallization at 150 C (1.3 C/s ramp).

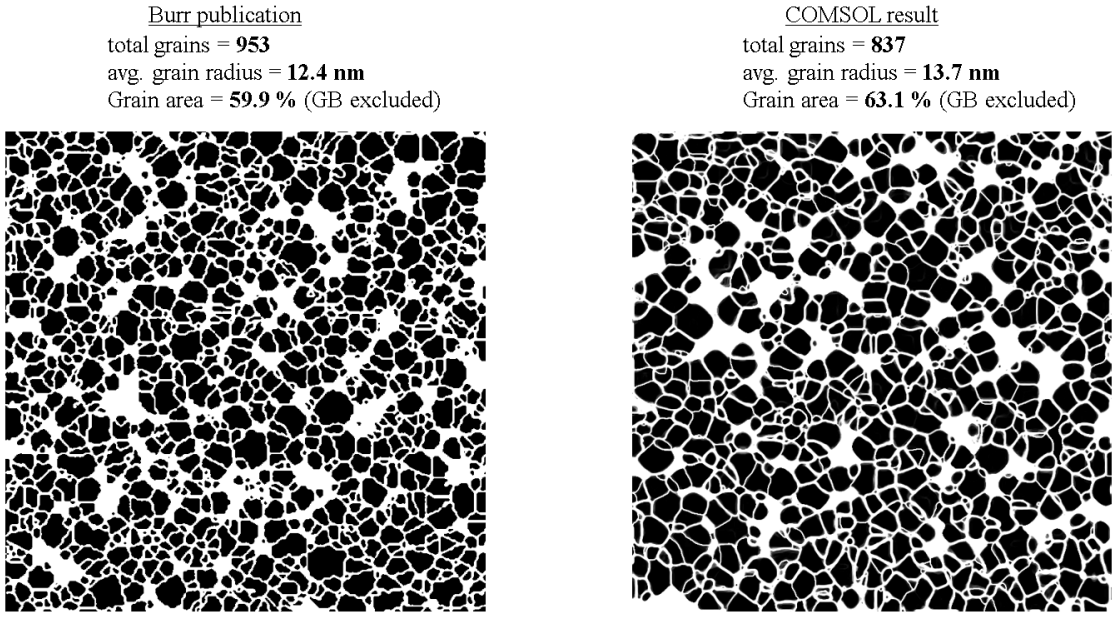


Figure 5.7 Model comparison for crystallization at 148 C (1.3 C/s ramp).

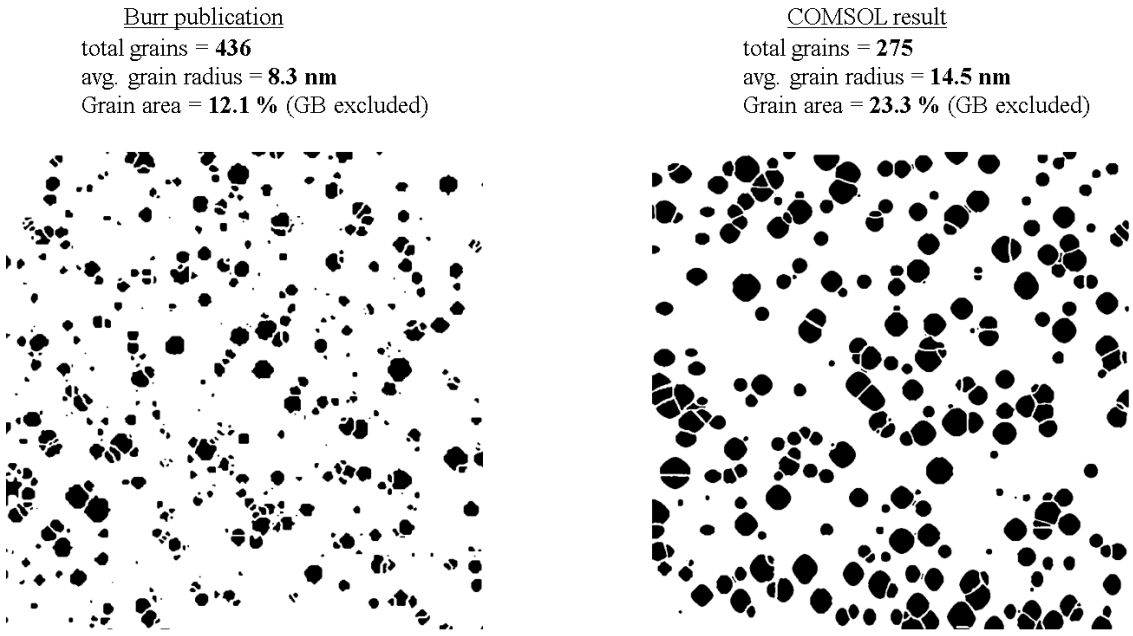


Figure 5.8 Model comparison for crystallization at 146 C (1.3 C/s ramp).

5.2 Incubation period

Nucleation probabilities are derived from the steady-state values published by Burr *et al.* [22], however according to the generally accepted view, the incubation time phenomenon [55-57] must be modeled for transient simulation conditions of as-deposited amorphous material. Melt-quenched amorphous material has been shown to crystallize very quickly due to the presence of quenched-in nuclei [57-59], whereas the as-deposited material requires additional time to overcome the thermodynamic barrier to nucleation in which the subcritical clusters become stable [55-57]. Temperature dependent incubation times for amorphous GST ($t_{inc}(T)$) have been reported in the literature by Wuttig et al. [57]. To capture this phenomenon in the model, an *incubation* variable is introduced to

keep track of the thermal history of each mesh point by integrating $t_{inc}(T)$ over time (Figure 5.9). The rate equation for the incubation variable is given by:

$$\frac{dIncubation}{dt} = (1-c)\left(t_{inc}(T)\right)^{-1} - (Incubation)(Step\_melt(T)) \quad \textit{eq (5.2)}$$

Here, step_melt(T) resets the *incubation* variable to 0 for mesh points whose temperatures greater than the melting temperature. We have slightly altered the behavior of $t_{inc}(T)$ in the high temperature range to continue reducing and to saturate at a minimum value of 20 ns close to the melting temperature, instead of turning around to begin increasing at 825 K. This change is made to allow the incubation variable to quickly increase when cooling from melt due to reflect the quenched-in nuclei and higher structural order of melt-quenched GST that is observed and reported in the literature [59, 60]. The *incubation* variable is used to scale the steady state nucleation probabilities when the incubation variable is less than 1, thus resulting in little to no nucleation of crystal grains until the thermodynamic barrier to nucleation is overcome.

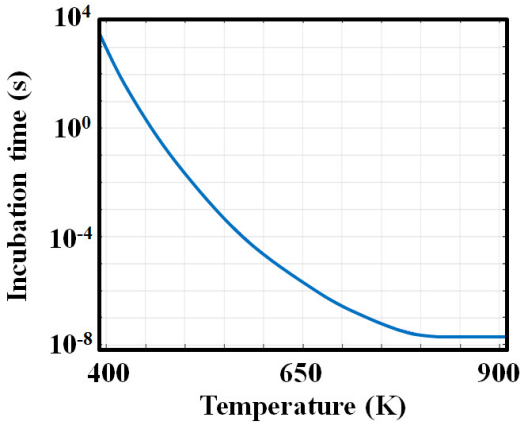


Figure 5.9 Incubation time vs. temperature curve used in the simulations, indicating the time for formation of sub-critical nuclei in the GST throughout the temperature range.

Figure 5.10 shows simulation results of a 25 nm crystalline GST film being melt-quenched by a 60 ns laser pulse ($T_{film} > T_{melt}$) and then subsequently annealed with a 100 ns, 35 mW green laser pulse, with sufficient time to cool to room temperature in between pulses. Details about the laser heating model are described in detail later in section 5.4. Figure 5.10(a) shows a small (< 5 nm) quenched-in nucleus that formed during cooling from the melt, and the amorphized spot width is ~ 320 nm. Nucleation and growth occurs quickly during the second laser pulse, where complete crystallization of the film occurs in ~ 100 ns. For comparison, we have simulated the crystallization of a 320 nm wide area in an as-deposited GST film with a longer 35 mW laser anneal, shown in Figure 5.10(b). Figure 5.10(c) shows the crystallization times of the melt quenched film and as-deposited film, ~100 ns and ~400 ns, respectively, which is in strong agreement with experimental data from the literature for melt-quenched and as-deposited GST films of similar thicknesses annealed with similar laser conditions [61]. The simulation results show that curves for the as-deposited and melt quenched cases have approximately equal slopes, hence similar nucleation and growth rates, but are shifted in time, capturing the incubation period phenomenon for the as-deposited film case. Temperature-time characteristics taken from the center of the GST film are shown in Figure 5.10(d). The temperature in the film during crystallization is higher for the as-deposited case, as the incubation time must be overcome, resulting in a slightly lower number of slightly larger grains due to the changes in nucleation and growth rates between these temperatures.

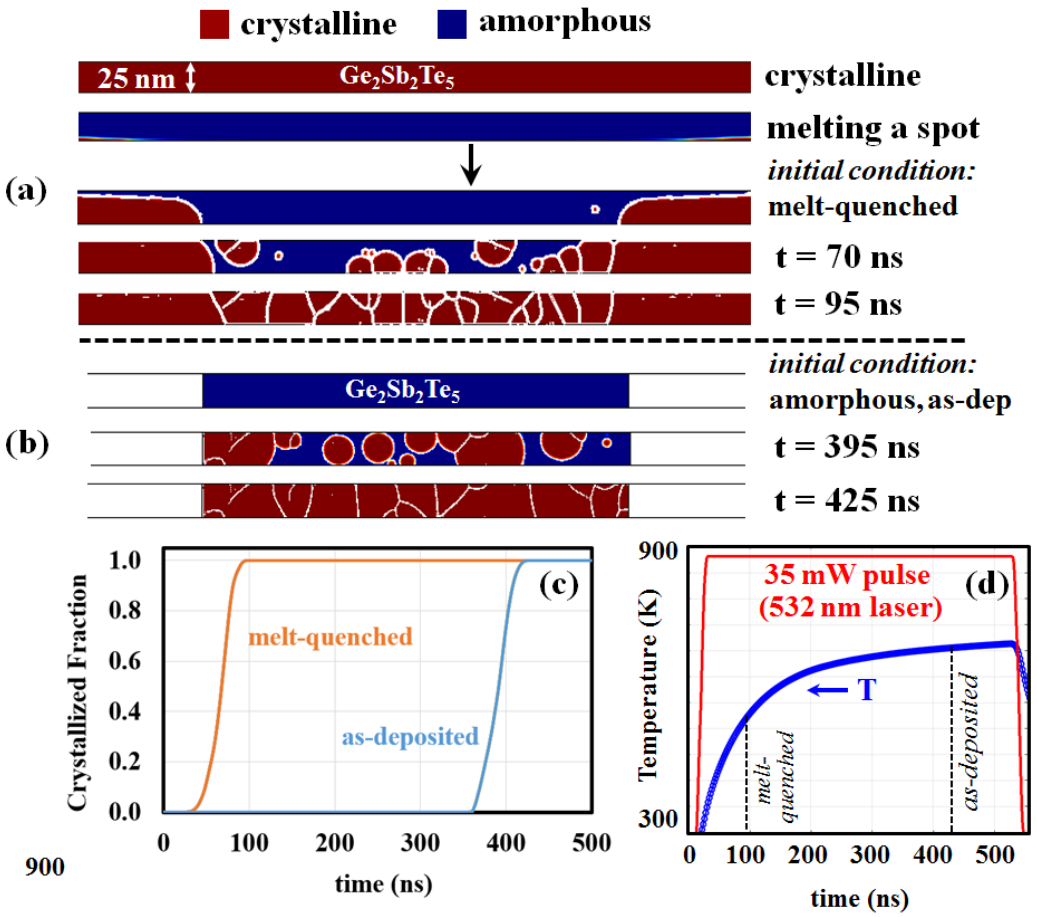


Figure 5.10 Simulation results comparing crystallization of a 25 nm GST film during a 35 mW green laser pulse (a) after melt-quenching and (b) as-deposited. (c) Crystallized fraction vs. time comparison. (d) Temperature vs. time characteristics during the laser anneal with dotted lines marking the crystallization times of the melt-quenched and as-deposited films.

5.3 Experiment

An experiment is performed to crystallize and "densify" the material in the cells to prevent excessive voids from forming during device operation, as the volume change between as-deposited amorphous and crystalline material is quite significant as previously mentioned in section 1.3. Here a laser annealing technique is used, opposed to

a conventional annealing in a furnace, to explore the effect of a large temperature gradient from the wafer surface and examine the possibility of crystallization starting from one end of the cell and localization of the voids. PCM cells are fabricated by IBM at the Watson Research center using SK Hynix design. Atomic layer deposition (ALD) is used to deposit amorphous X-doped $Ge_XSb_YTe_Z$ for the cells (GST_{ALD}). Material composition (X, Y, Z components), device dimensions, and fabrication process steps cannot be disclosed as it is proprietary information belonging to IBM and SK Hynix, respectively. Transmission electron micrograph (TEM) of an as-fabricated amorphous device is shown in Fig 5.11(a). A 532 nm (green) laser is modulated and scanned across the field of PCM cells, and the laser annealing of the PCM cells is performed by Ultratech. The laser spot in the experiments is ~ 10 μm in the direction of the scan and ~ mm wide in the orthogonal direction to the scan. The laser is pulsed for 50 ns durations with a frequency of 10 kHz at a scan rate of 167 mm/s. The substrate is held at ~ 525 K and laser pulses with energy per area of ~ 1.589 mJ/mm^2 are delivered to the wafer. Experimental results from a single scan are shown in Fig. 5.11(b,c), and from 5 scans shown in Fig. 5.11(d,e). Cells that experience a single scan are partially crystallized with ~ 25% crystal fraction, and are typically fully crystallized after experiencing multiple scans. Crystal planes of the individual grains can be seen with higher magnification TEM, however cannot be shown here due to the confidentiality of the cell size.

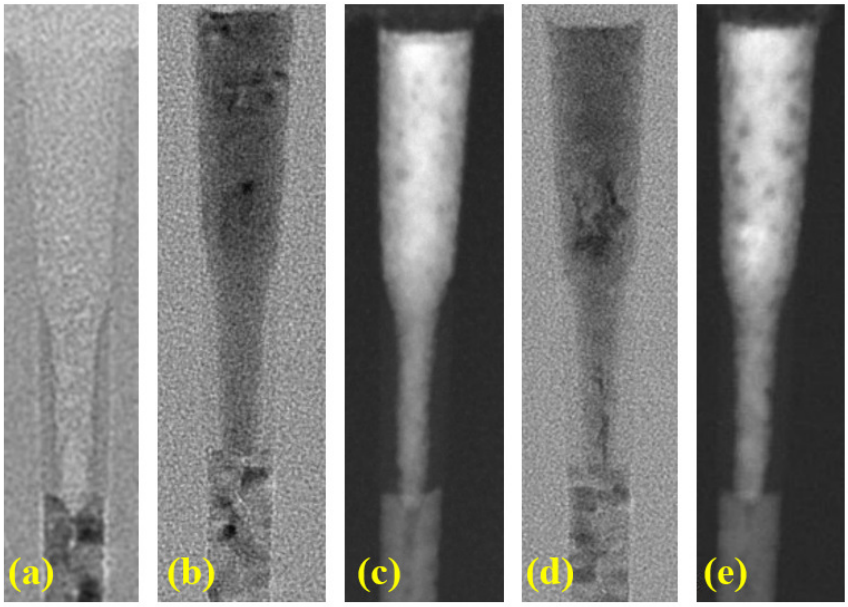


Figure 5.11. (a) TEM of an empty pore cell structure. (b) TEM and (c) STEM of cells annealed with a single laser pulse, and (d) TEM and (e) STEM of cells annealed with multiple laser pulses.

STEM images shown in Fig 5.11(c,e) show the void locations that occurred during the first-time crystallization of these cells for the single and multiple scan cases, with larger and more apparent voids appearing in the multiple scan case. Simulation results, discussed later in this manuscript, predict that the wafer surface is approximately equal to the melting temperature of the phase-change material, however the cells are below the melting temperature due to the nature of laser heating (strong thermal gradient along the depth of the wafer). Thus we expect there is not any significant melting of the cells during the laser anneals. Figure 5.12 highlights void locations for the single and multiple scan cases and the area fraction and number density of the voids in various cells, obtained using image processing software (Appendix 8.4). Cells in the single scan case have less void area than the multiple scan case, as expected since there is less

crystallization and thus less volume change in the material. However, the number of voids observed in the two cases is approximately the same. This may be due to several close-by small voids coalescing together into a larger void, as previously observed in GST [62], as well as single voids becoming larger as the grains grow due to the volume change and increased strain resulting from crystalline GST having a higher Young's modulus than amorphous GST [63].

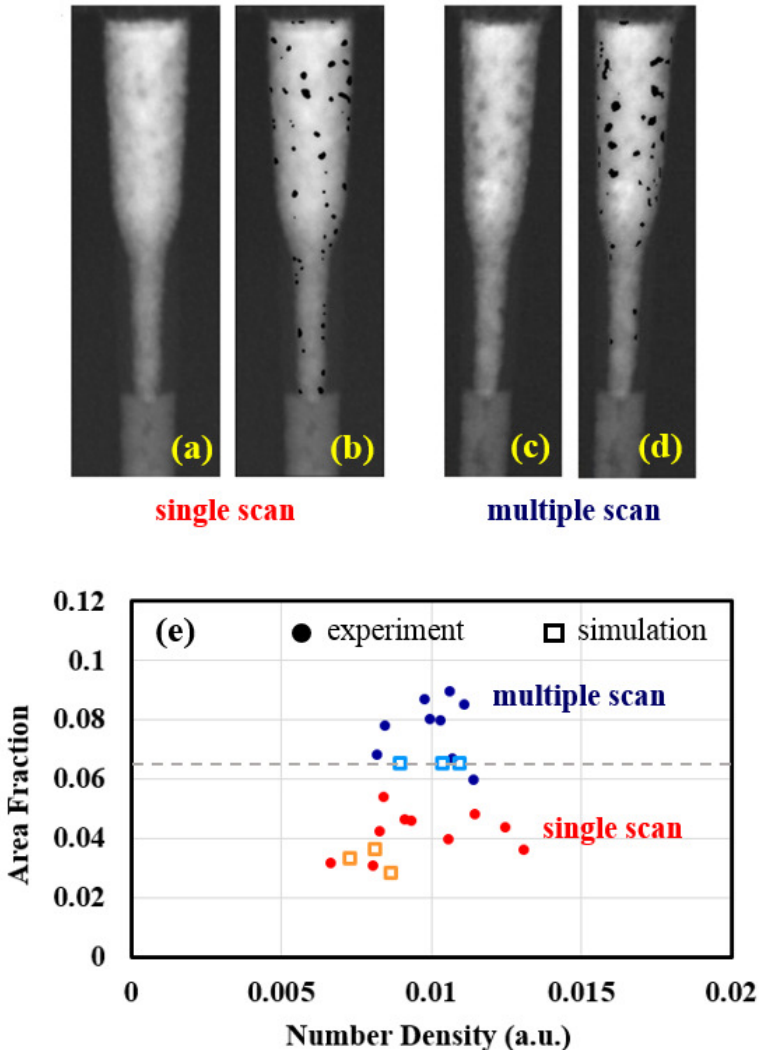


Figure 5.12 STEM images of laser annealed cells in (a) the single scan case with (b) highlighted void areas, and (c) the multiple scan case with (d) highlighted void areas. (e) Distribution of area

fraction and number density of voids in the cells from the experiment, as well as simulation results using the model later discussed in section 5.5. The dotted line marks indicates 0.065 void area fraction, which corresponds to the ~6.5% density change in the material that the model is designed to achieve as the crystal fraction reaches 100%.

5.4 Laser Model

The laser anneals from the thin film crystallization simulations are modeled with a heat source that is a function of space and the absorption and reflection coefficients of the materials:

$$Q = Q_0 \cdot (1 - R_C) \cdot \frac{A_C}{\pi \cdot \sigma_x} e^{-\frac{x^2}{2\sigma_x^2}} \cdot e^{-A_C \cdot y} \qquad \textit{eq (5.3)}$$

Where y is the distance from the surface of the wafer into the substrate x is the distance from the center of the laser spot, *d* is the assumed depth of the 2-D planar simulation (10 nm), A_C is the absorption coefficient, R_C is the reflection coefficient, and σ_x is the standard deviation of the laser power distribution in the x direction (σ_x = 1 μm used in the thin film simulations). Parameters A_C and R_C for amorphous and crystalline GST corresponding to the 532 nm wavelength of the laser are shown in Table 5.1. A_C and R_C values used for TiN, SiO_2, and Si at this wavelength are 2.8 x 10^7 m^{-1} and 38%, 50 m^{-1} and 5%, and 3 x 10^5 m^{-1} and 34%, respectively. The value for Q_0 during the crystallization anneal is 35 mW, a typical power level for laser crystallization experiments with a similar wavelength laser, which heats the film to ~ 600 K where the nucleation rate in GST is maximized. A 75 mW pulse is used to melt a small spot of GST with a 60 ns pulse.

	GST_{225} Material Properties	Amorphous	Crystalline (FCC)
Thermal	Heat Capacity (J / kg·K)	202*	202*
	Thermal Conductivity (W / m·K)	0.2	~ 0.5 - 1.7 (T-dep.)
	Density (kg/m^3)	5870	6270
Mechanical	Coefficient of Thermal Expansion x 10^{-6} (1/K)	13.3	17.4
	Poisson Ratio (unitless)	0.275	0.255
	Young's Modulus (GPa)	24.8	39.5
Optical	Absorption Coefficient (1/m)	5×10^7	1×10^8
	Reflection Coefficient (%)	42	51

Table 5.1 All material parameters used for amorphous and crystalline GST in the simulations [41-43, 63-65]. *A large spike in heat capacity at the melting temperature is included to model the latent heat of fusion, shown in further detail in Ref [39]. Temperature dependent thermal conductivity can also be seen in Ref [37].

The laser anneals of the PCM cells are modeled similarly as heat source, however the Gaussian distribution term in the lateral direction is dropped as the laser spot size is significantly larger than the devices and simulation area:

$$Q = Q_0 \cdot (1 - R_C) \cdot \frac{A_C}{X \cdot d} \cdot e^{-A_C \cdot y} \qquad \textit{eq (5.4)}$$

Power distribution is uniform based on the energy/area figures used in the experiments:

$$Q_0[W] = \frac{energy}{area}\left[{}^{J}/_{m^2}\right] \cdot \frac{1}{t_{pulse}}\left[{}^{1}/_{s}\right] \cdot X \cdot d\ [m^2] \qquad \textit{eq (5.5)}$$

where X is the total width of the simulation area (10 µm). Since the laser spot size is very large in comparison to cell dimensions, along with the very low duty cycle and relatively

low frequency of the laser modulation (0.05% ON time, 100 µs between pulses), the laser anneal is modeled as a stationary 50 ns rectangular pulse with 10 ns rise and fall times. A single cell is meshed heavily with a mesh size on the order of 1 nm^2 and the crystallization and void formation models are applied that cell, as additional heavily meshed cells result in excessively large simulation times and file sizes. A simulation result of the laser anneal from the experiments is shown in Fig 5.13, showing large temperature gradients in the PCM cells as a result of the large absorption coefficient of GST and the exponential decay behavior of the heat source in the *y* direction.

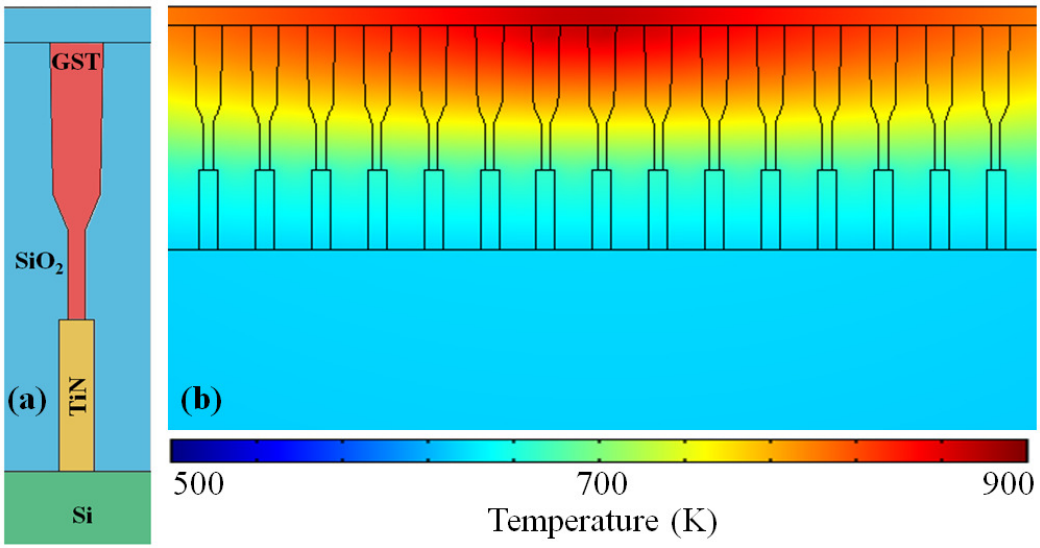


Figure 5.13 PCM cell materials and geometry (left), temperature profile of the wafer during the peak temperature in the laser anneal.

Although the cells are not expected to be melting in the experiments, simulations are performed to explore the temperature in the cells for higher laser powers that would cause melting to occur. When melting an entire cell with laser heating, the temperature at

the top of the cells becomes significantly higher than the melting temperature due to the large temperature gradients that occur during laser heating. The effects of substrate temperature and laser pulse width are shown in Figure 5.14. More extreme temperature gradients are observed for faster pulses and lower substrate temperatures.

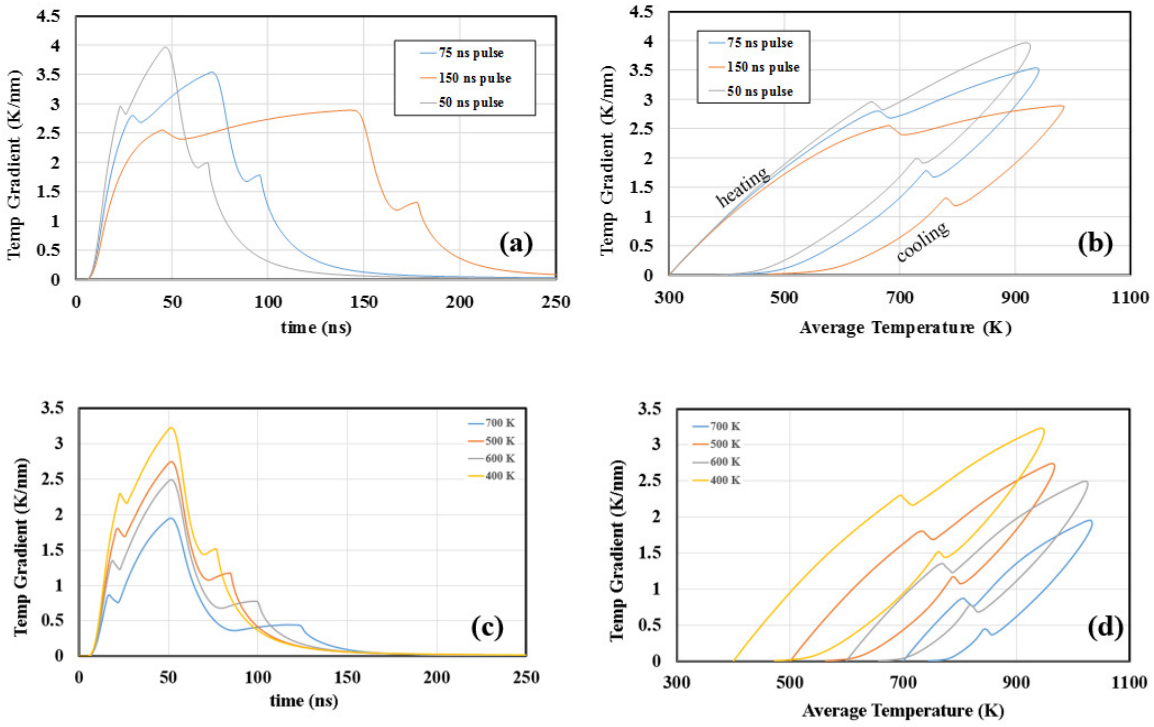


Figure 5.14 (a) Temperature gradient vs. time and (b) temperature gradient vs. average temperature in a PCM cell for three different pulse widths, where the maximum temperature in the cell for each case is 1200 K. (c) Temperature gradient vs. time and (d) temperature gradient vs. average temperature in a PCM cell for four different substrate temperatures. In all curves, the "bumps" seen in the heating and cooling correspond to the melting and re-solidfying of the cells.

5.5 Void Formation Model

The confined PCM cell is a very attractive design for a PCM cell due to its reduced reset current, small device pitch, and multi-bit storage capabilities. However, there are several fabrication challenges and reliability issues which hinder the commercialization of this technology. These issues stem from the volume difference between the different phases of GST material – especially between the as-fabricated amorphous phase and the crystalline phase [64] – resulting in void formation which may lead to device failure. Developing a fabrication technique for confined cells that promotes device reliability (i.e. void-free crystallized cells) is of critical importance. However, the significant volume change between amorphous and crystalline GST and the stochastic nature of crystal grain nucleation leads to disseminated void formation within the device, as observed in the experiments (Fig 5.12). Here, we present a model for the crystallization and void formation during the laser annealing experiments.

A solid mechanics model is included into the COMSOL Multiphysics simulation to calculate the stress within the material as it is heating and crystallizing. Mechanical properties of amorphous and crystalline GST_{225} are shown in Table 5.1. The respective values for coefficient of thermal expansion, Poisson ratio, and Young's Modulus used in the model are 7.1 x 10^{-6} K^{-1}, 0.199 and 676 GPA for TiN, 0.55 x 10^{-6} K^{-1}, 0.17 and 73.1 GPA for SiO_2, and 2.6 x 10^{-6} K^{-1}, 0.28 and 170 GPA for Si. It has been reported in the literature that the volume reduction of the crystalline phase results in deformation of the material leading to dislocations and increased stress, especially at grain edges [66, 67]. Additionally, stress induced void formation in other polycrystalline materials typically occurs at the grain boundaries [68, 69]. Hence, void formation in our model occurs once a

significant amount of crystallization has taken place (> 15%) at grain boundaries or the sidewall interfaces. Specific locations for the formation of voids on the grain boundaries are determined using a stochastic process similar to the crystal grain nucleation algorithm, but in this case the probability of occurrence is determined by the von Mises stress (indicating distortion energy) rather than temperature. Existing voids expand at a rate based on the relative von Mises stress in the material as well as the rate of crystallization, as the volume reduction in the crystallized material is the driving force behind the void formation. Similar to the crystallization modeling method, a void variable $\boldsymbol{\varphi}$ represents a void or non-void location with a value of 1 or 0, respectively, and the rate equation is given by:

eq (5.6)

$$\underbrace{\frac{d\varphi}{dt}}_{\text{void rate}} = \underbrace{f_{nuc}(c, \varphi, \text{GB})}_{\text{void formation occurs at grain boundaries as grains grow together}} + \underbrace{\nabla\left[f_{growth}(c, \varphi, \sigma) \cdot \nabla\varphi\right]}_{\text{existing voids grow at a rate proportional to stress and crystallization rate}} + \underbrace{f_{stability}(c, \varphi)}_{\text{maintains } 0 < \varphi < 1 \text{ and conservation of mass}}$$

where σ is the von Mises stress. The rate equation achieves and maintains the relationship $\varphi_{avg} = c_{avg} \cdot 6.5\%$ in the PCM cell domain to satisfy the law of conservation of mass as the GST is crystallizing.

Estimated nucleation and growth rates for the GST_{ALD} are used in the simulations that model the experiment (Figure 5.15). The GST_{ALD} material does not begin to crystallize in the order of minutes until a temperature of ~ 575 K, which is ~150 K higher than what is observed in GST_{225} (~ 425 K). In the experiments, the chuck temperature of

525 K would be sufficient to crystallize $Ge_2Sb_2Te_5$ (GST_{225}) material, however it does not crystallize the GST_{ALD} material. The nucleation probability curve for GST_{ALD} is estimated by shifting the curve for GST_{225} by 150 K and scaling it to also drop off before the melting temperature. Additionally, dopants added to the GST are shown to significantly slow down crystallization speed [60, 61], hence the growth rate of the GST_{ALD} is estimated by scaling the curve for GST_{225} by an order of magnitude. These estimated rates give simulation results of crystallized fraction and number of grains that are in good agreement with experimental observations.

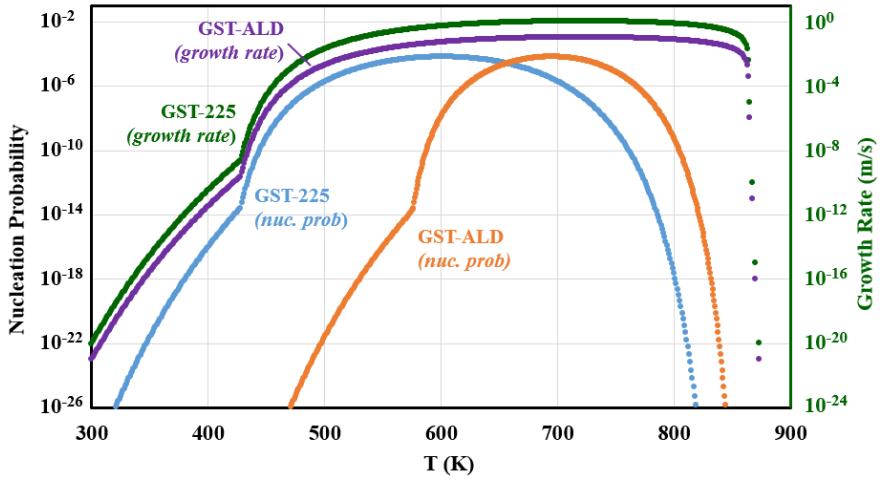


Figure 5.15 Nucleation probabilies derived from the nucleation rates for PVD GST_{225} [22] (blue) and estimated for the GST_{ALD} (orange), corresponding to 5 ns time intervals and a 1 nm^2 2-D mesh with 10 nm depth in a 2-D planar simulation. Growth velocity for GST_{225} (green) taken from [22] and estimated for GST_{ALD} (purple).

Simulation results of crystallization and void formation during the laser anneal are shown in Figure 5.16, alongside experimental results for comparison. Figures 5.16(c,d)

illustrate how void formation is captured in the model, as the voids occur at the grain boundaries of the initial grains in the cell that are growing into each other. Figures 5.16(d-f) show the evolution of crystallization in one cell across multiple scans and the expansion of existing voids as well as formation of new voids that occur during crystallization. The simulation results of void formation in the fully crystallized cells (Figures 5.16(f-h)) from the multiple scan case strongly resemble the STEM image of the cells from the experiment, and the model is capturing the general phenomenon that is taking place. A comparison between experimental and simulation results for area fraction and number density is shown previously in Figure 5.12(e). A comparison between the simulation and TEM images of experimental results is shown in Figure 5.17, which more clearly highlights the crystallinity in the cells from the experiments. It is more difficult to directly compare crystallization for simulation and experiment for the multiple scan case because of the way the laser is pulsed and scanned (fast pulse time, slow scan rate, low pulse frequency) – each cell may not have received a pulse for every scan, or in some cases pulses with reduced power if they happened to be away from the laser spot center. Thus, the results from the single scan case are more directly comparable.

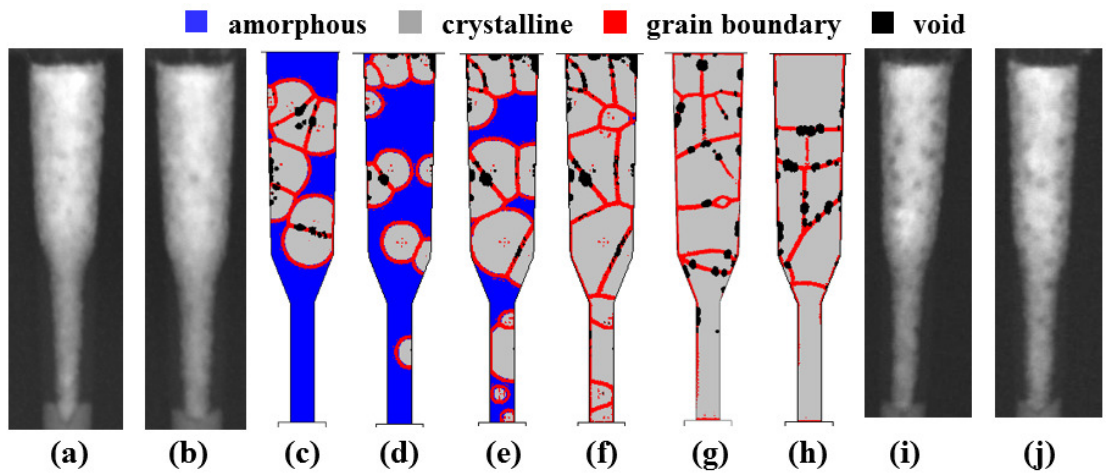


Figure 5.16 (a,b) STEM image of cells for the single scan laser anneal. (c,d) Simulation result of crystallization and void formation in cells for the single scan case. (e) Simulation result of the same cell shown in (d) after a second scan, and (f) after a third scan. (g,h) Additional simulation results of cells for the multiple scan laser anneal, alongside (i,j) STEM images of cells for the multiple scan case for comparison.

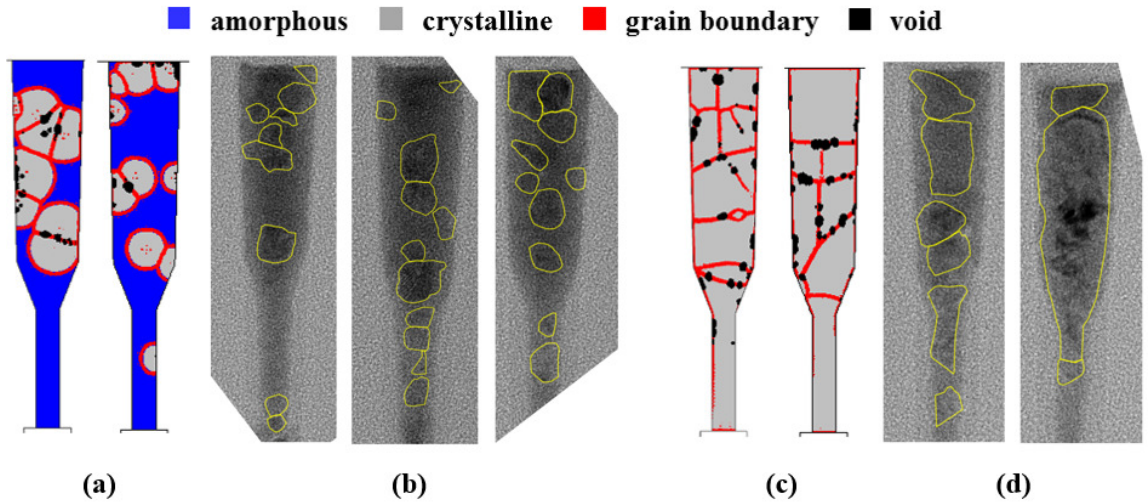


Figure 5.17 (a) Simulation result and (b) TEM images showing experimental result of cells for the single scan laser anneal. (c) Simulation result and (d) TEM images showing experimental result

of cells for the multiple scan laser anneal. In the TEM images, crystal grains are shown with a yellow outlined, determined from higher magnification inspection from high resolution TEM.

This model offers the flexibility and capability to simulate the crystallization of an arbitrary shaped GST nanostructure during any annealing conditions or electrical device operation, including the void formation that occurs due to volume reduction in the material.

6. Device Fabrication

A joint study agreement with the phase change memory group at IBM has enabled our group to fabricate GST nanostructures at the Watson Research Center in Yorktown Heights, New York. Various wafers with patterned GST nanostructures or uniform GST films are being fabricated, allowing us to study melting and crystallization of GST and measure material parameters at high-temperatures, such as Seebeck coefficient and liquid resistivity. Three lots of wafers have been fabricated (each lot consisting of approximately 8 wafers):

- *PCMUCRTM04*: Uniform GST film over large patterned W contacts
- *PCMUCONOXL22*: Patterned GST nanostructures on SiO_2 substrate, with W or TiN metal contacts
- *PCMUCONI2L41*: Patterned GST nanostructures on Si_3N_4 substrate, with W or TiN metal contacts

In each of the lots, 600 nm – 1 μm of thermal oxide is grown on a Si substrate to provide electrical and thermal isolation between the device structures and the substrate. In one lot, PCMUCONI2L41, an additional thin film of Si_3N_4 is deposited on top of the oxide. Trenches for bottom electrode contacts are defined and etched using photolithography and reactive ion etch (RIE) processes. Chemical vapor deposition and physical vapor deposition processes are used to fill the trenches with metal. For the two lots with patterned nanostructures, a chemical-mechanical polish (CMP) is performed to remove the excess metal and planarize the wafer surface. GST films of 20, 50, and 100 nm, are sputtered on the various wafers of each of the lots, and the films are capped with 15 nm

SiO_2. A final lithography and RIE step is performed on PCMUCONOXL22 and PCMUCONI2L41 to define the GST nanostructures. Selected wafers from these two lots are dipped in HF to achieve suspended wires by undercutting the substrate under the structures. Appendix 8.5 illustrates the fabrication steps of the nanostructures in detail. Figure 6.1 shows various images of devices from the lots.

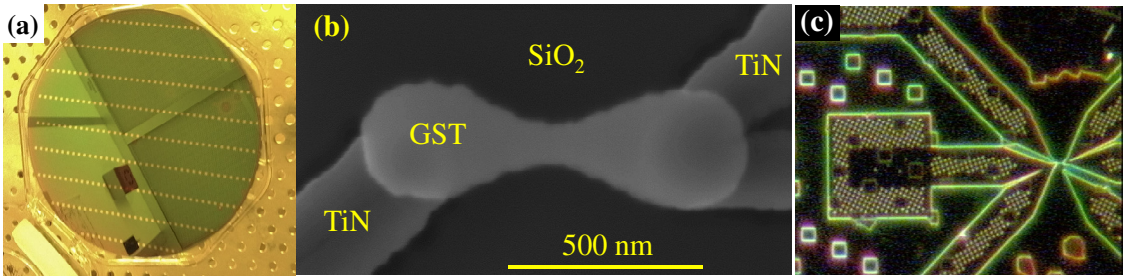


Figure 6.1 (a) Photograph of an 8 inch wafer from PCMUCRTM04 showing the array of large patterned W contacts in SiO_2, just prior to GST film deposition. (b) SEM image of a GST nanostructure on a completed wafer from PCMUCONOXL22. (c) Dark-field optical microscope image of a device on a completed wafer from PCMUCONOXL22 after etching with HF for wire suspension.

7. Conclusion

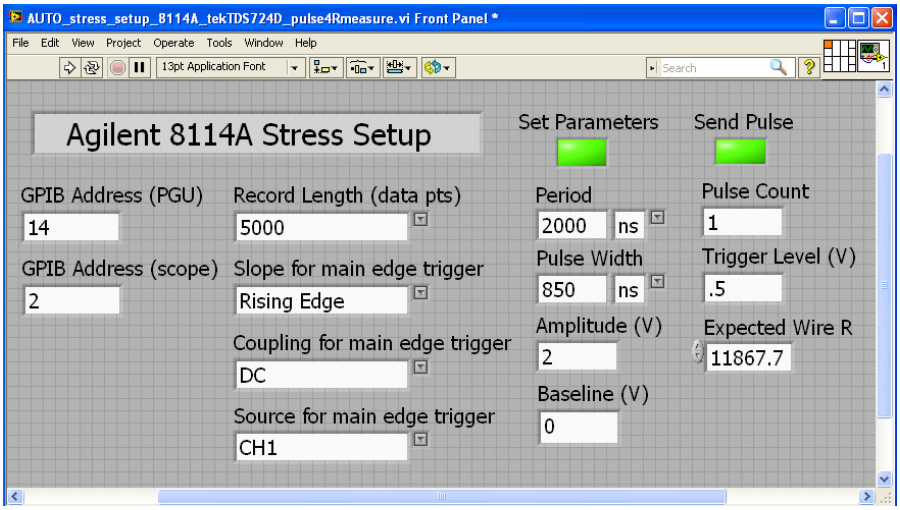
In summary, a new and interesting phenomenon of solid-liquid phase change oscillations in a Si micro-/nano-wire is observed and a US patent application (US20110304404 A1) is filed for a device concept utilizing this phenomenon. Scaling behavior of the device concept is estimated using simulation techniques and it is shown how frequency can be controlled or tuned by various parameters. Simulation results also suggest that for wire lengths on the nanometer scale, faster melting of the nanowire can occur due to the electrical breakdown of silicon and oscillation frequencies may exceed 1 GHz.

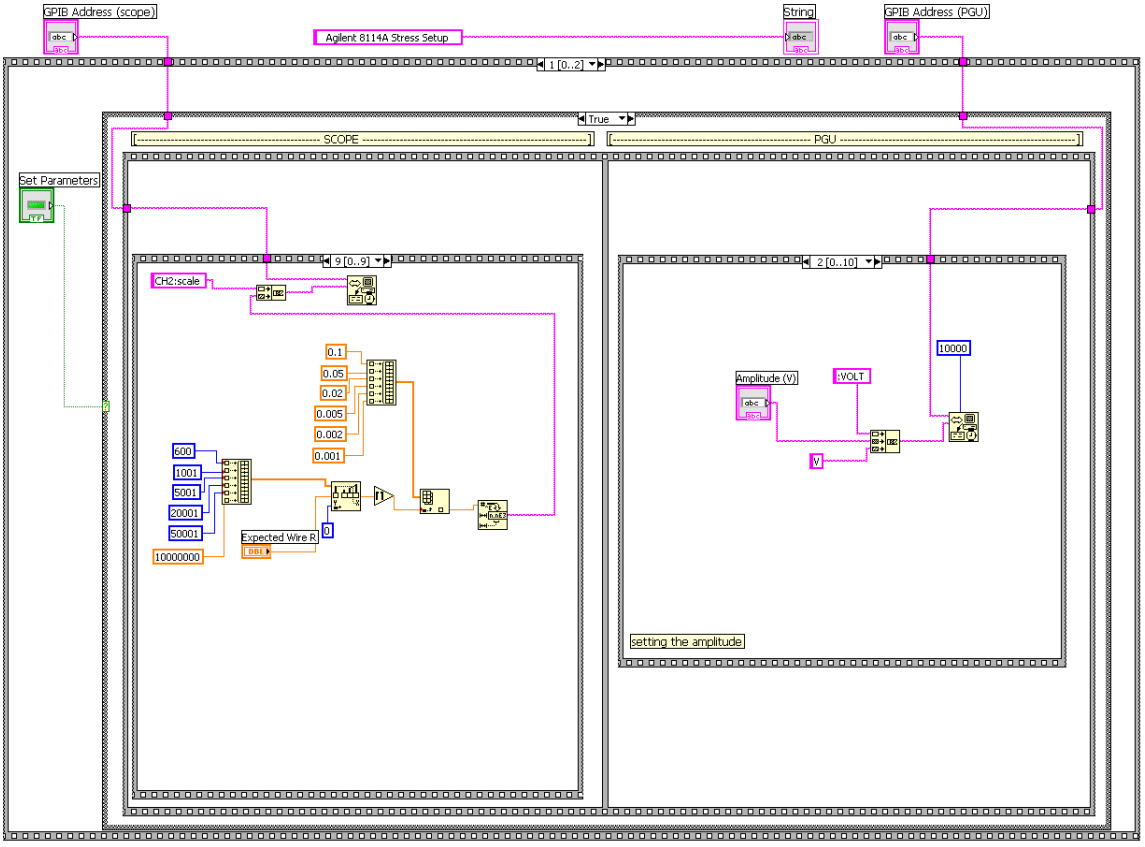
Additionally, electrical performance of PCM devices with various geometries and load conditions is analyzed using finite element modeling with temperature dependent parameters, and demonstrated the importance of load conditions and effects of variations in device geometry. A model for crystallization of GST, which is able to simulate the crystallization of an arbitrarily shaped GST nanostructure during any annealing conditions or electrical device operation, is developed in collaboration with fellow group member Zachary Woods. The crystallization model is built upon by incorporating a model for void formation, as the density change between amorphous and crystalline phases can result in void formation during crystallization. This model offers the utility of capturing various nanoscale phenomena such as incubation, nucleation, growth and void formation in GST, and offers the flexibility to be integrated into simulations of fabrication process steps or of electrical device performance. Simulation results from the model closely agree with various experiments done at IBM and elsewhere in the literature.

8. Appendix

8.1 LABVIEW controls for measurement equipment

Pulse Generator control:

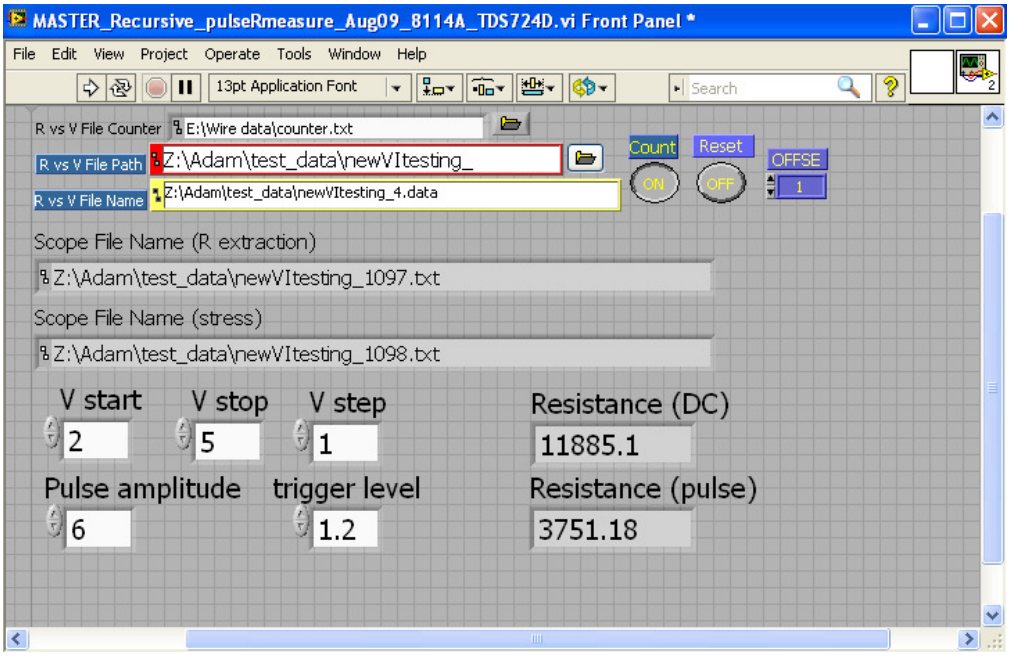




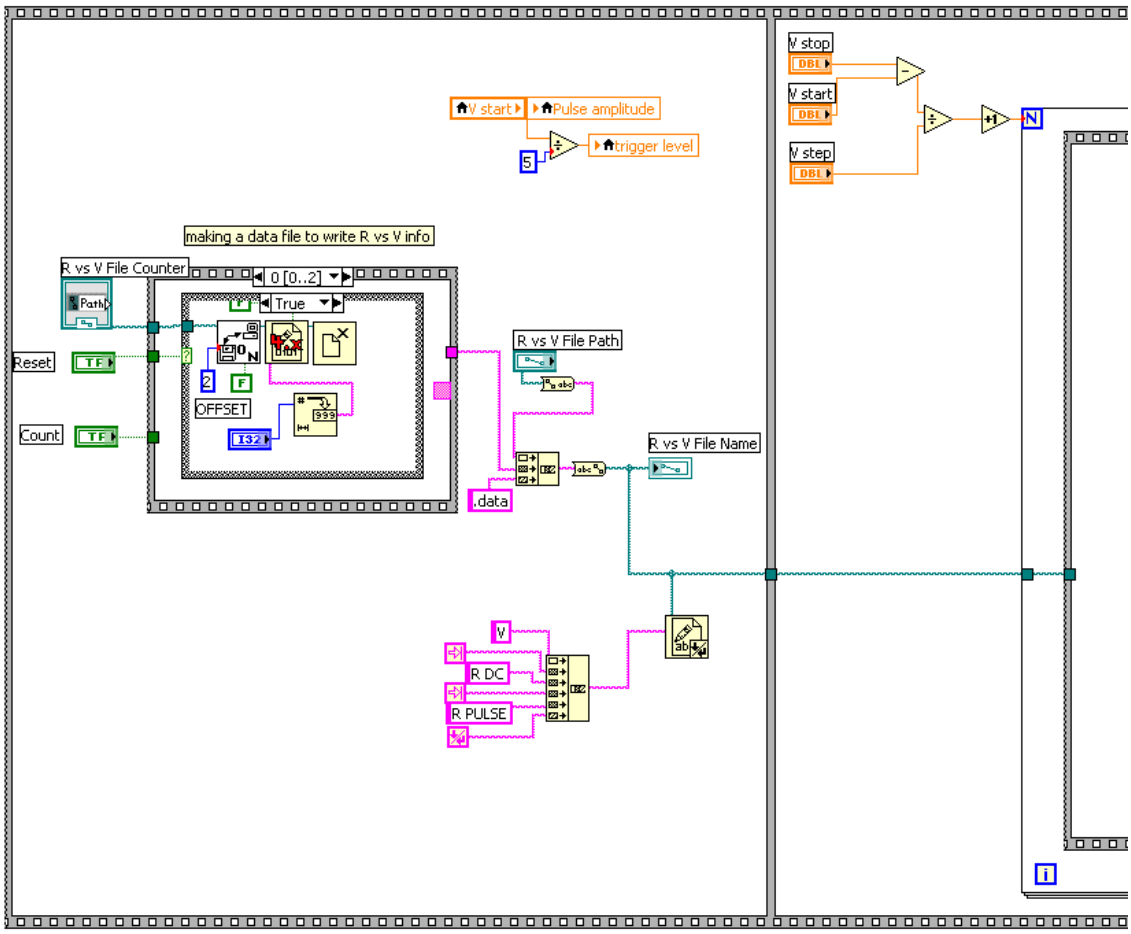
This code programs the pulse and adequately adjusts the oscilloscope scales. It also acquires and plots the data from the oscilloscope. The button “Set Parameters” sends the parameters from the labview controls to the equipment, and the “Send Pulse” button will allow the pulse generator to

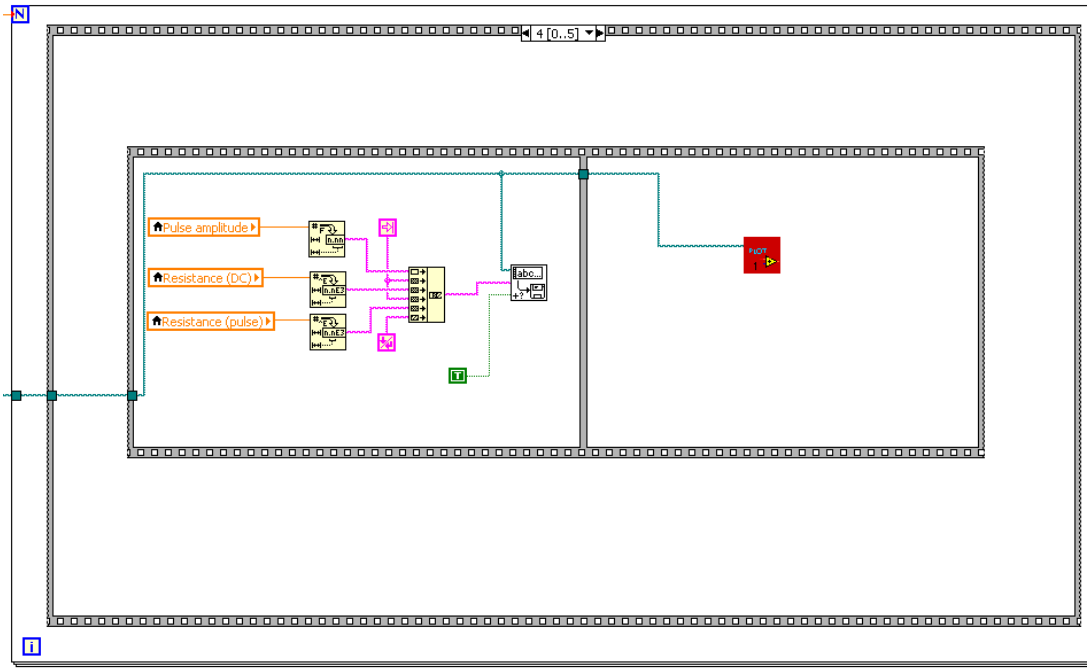
deliver the electrical pulse. With the “Set Parameters” button on and the “Send Pulse” button off, the VI can be run to just program the equipment without sending any pulses. This VI allows the user to set the amplitude and timescale of a rectangular electrical pulse, and also can set the oscilloscope vertical scale based on expected wire resistance.

Repeated Incrementing voltage pulse with resistance measurements before and after:



This VI controls the pulse generator VI shown above, as well as additional VIs to allow for experiments with repeated pulses with incrementing amplitude, as seen in Figure 2.2. “V start” is the voltage amplitude of the first pulse to be sent, “V stop” is the voltage amplitude of the final pulse to be sent, and “V step” controls the increment in amplitude between each pulse. Timescales of the pulses can be set from the pulse generator control VI. This VI records the resistance of the wire during each pulse (minimum resistance with small moving average to reduce noise influence), and after each pulse with a low amplitude long duration pulse. The data is saved into an “R vs V” file, and the oscilloscope data from each pulse is saved to separate files. Only the pulse generator and oscilloscope are used for these measurements (Agilent 8114A Pulse Generator and Tektronix TDS724D Oscilloscope). The back panel of the VI is shown below:


V start
Pulse amplitude
5
trigger level
V stop
V start
V step
DBL
making a data file to write R vs V info
R vs V File Counter
0 [0..2]
Path
True
Reset
TF
2
F
OFFSET
I32
Count
R vs V File Path
.data
R vs V File Name
V
R DC
R PULSE


4 [0..5]
Pulse amplitude
Resistance (DC)
Resistance (pulse)

8.2 MATLAB crystallization code

The block diagram that illustrates the algorithm for the 2-D function DCM(x,y,t,T) is shown in Figure 5.3. The code for the function is given here. This DCM function is called at each timestep or intermediate timestep of COMSOL's iterative solver. The inputs are to the function are the *x* and *y* coordinates of all the mesh points being solved for, the time *t* in the simulation, and the temperature *T* at each mesh point. Crystal grains or nuclei are formed using a probability function based on the temperature dependent nucleation rates, and the grains are grown using a temperature dependent growth rate. This code creates an object array for each grain formed with various details about the grains, such as the time when it first appeared, the location where it first appeared, the radius, the points most recently added (grain edges), and a list of all points belonging to that grain. The output is an array of c values of 0 or 1 (amorphous or crystalline), corresponding to all the mesh point locations in *x* and *y*.

```
function out = DCM_2D(x,y,t,T)

    % COMSOL coordinates come in as [m]
    % Converting units into [nm] for algorithm
    x = 1e9.*x;
    y = 1e9.*y;

    e = 0.01;



 %   indeces of the boundary points
 %   bounds =  [ find(abs(x_grid - 0) < e  |  abs(x_grid - 15) < e );
find(abs(y_grid - -100) < e  | abs(y_grid - -25) < e ) ];
 %   bounds =  [ find(abs(x_grid - 15) < e ); find(abs(y_grid - -100) <
e ) ];
 %   mult = 1;

START = 0;
load('R:\DCM\START.mat');


    if (START == 1)
         % Loading variables from previous timestep
         load('R:\DCM\DCMn.mat');
         load('R:\DCM\grids_2D.mat');
    else
         % Load INITIALIZATION variables for t=0
         load('R:\DCM\DCM0.mat');

         % Generate MATLAB grid of regular spacing
        x_coords = [-50:1:50]';
        y_coords = [-30:1:-15]';
        for i = 1:length(y_coords)
            x_grid(1+(i-1)*size(x_coords,1):i*size(x_coords,1),1) =
x_coords;
```

```
            y_grid(1+(i-1)*size(x_coords,1):i*size(x_coords,1),1) =
y_coords(i);
        end


        save('R:\DCM\grids_2D.mat', 'x_grid', 'y_grid');

         c = zeros(size(x_grid,1),1); % crystal map for first time step
         c_results = c;

         %R is 'Results' variable
         % R = 0 while code is computing during COMSOL simulation
         % R = 1 after simulation is finished for plotting results in
         %       COMSOL
         R = 0;
         save('R:\DCM\DCMR.mat','R');

         % COMSOL runs the same timestep many times over for different
         % sections of the geometry. The bank variable will accumulate
the
         % different sections of x-y points that belong to the same
         % timestep
         bank(1).x = [];
         bank(1).y = [];
         bank(1).T = [];
         bank(1).t = [];

         % ASSIGN c_interp HERE
         c_interp   = fit([x_grid y_grid], c, 'nearestinterp');

         START = 1;
         save('R:\DCM\START.mat','START');

    end

    % Set results variable to 1 at the last timestep of the simulation
    if(t(1) >= 99999)
        R = 1;
        save('D:\DCM\DCMR.mat','R');
    else
        R = 0;
    end

    % Load results variable
    load('R:\DCM\DCMR.mat');

% Execute N & G Algorithms only for R = 0
if (R == 0)

    %UNIQUE TIMESTEPS ONLY
    if (t(1) > t_previous)

        % Interpolation of COMSOL T onto our MATLAB xy space
```

```
        T_map = fit([bank(length(t_track)).x bank(length(t_track)).y],
bank(length(t_track)).T, 'biharmonicinterp');

        % calculating time difference between unique timesteps
        delta_t    = t(1) - t_previous;

        T_grid = T_map(x_grid,y_grid);

        % GROWTH
        % Temperature dependent growth rate interpolated onto MATLAB xy
        if ~isempty(g(1).nucleus)  % if nucleation has occured, execute
growth code.
            GR_grid = GrowthRate_T(T_grid);
                for N = 1:length(g)

                    if isempty(g(N).recentlyadded)
                     %GR from last point in allpoints
                        GR = GR_grid(intersect(find([x_grid] ==
g(N).allpoints(size(g(N).allpoints,1),1)), find([y_grid] ==
g(N).allpoints(size(g(N).allpoints,1),2))));
                     else
                     for M = 1:size(g(N).recentlyadded,1)
                        GR_edges(M,1) = GR_grid(intersect(find([x_grid]
== g(N).recentlyadded(M,1)), find([y_grid] ==
g(N).recentlyadded(M,2))));
                     end
                     GR = mean(GR_edges);
                    end

                    g(N).radius = g(N).radius + 1e9.*GR.*delta_t;
                    g(N).recentlyadded = [ ];

                    rad_check = ((x_grid - g(N).nucleus(1)).^2 +
(y_grid - g(N).nucleus(2)).^2) - (g(N).radius)^2;
                    would_grow = ceil(rad_check./-1000000);
                    will_grow = would_grow - c;
                    Growth_Sites = find(will_grow == 1);

                    for k = 1:length(Growth_Sites)
                        j = Growth_Sites(k);

                        % add point into the grain w and global c
variable
                        g(N).allpoints = [g(N).allpoints; x_grid(j)
y_grid(j)];
                        g(N).recentlyadded = [g(N).recentlyadded;
x_grid(j) y_grid(j)];
                        c(j,1) = N;
                    end
                end
        end



        % NUCLEATION
```

```
        p_compare   = rand(size(x_grid));
        NR_grid = NucleationRate_T(T_grid);
        p_grid =  NR_grid.* delta_t .* (1e-9) .* (1e-9) .* (20e-9);

        success = ceil(p_grid - p_compare);
        Nucl_success = success - c;
        Nucleation_Sites = find(Nucl_success == 1);

        for f = 1:length(Nucleation_Sites)
            j = Nucleation_Sites(f);

        if (max(c) == 0) %% if first grain
                    %  initialize structure for grain organization and
denote
                    %  first grain c = 1
                    g(1).nucleus       = [x_grid(j) y_grid(j)];
                    g(1).allpoints     = [x_grid(j) y_grid(j)];
                    g(1).recentlyadded = [x_grid(j) y_grid(j)];
                    g(1).radius        = [0];
                    g(1).birthday      = t(1);
                    c(j,1)             = 1;


                else    %% for additional grains
                    %  incrementing structure index and c variable
                    g(max(c)+1).nucleus         = [x_grid(j)
y_grid(j)];
                    g(max(c)+1).allpoints       = [x_grid(j)
y_grid(j)];
                    g(max(c)+1).recentlyadded   = [x_grid(j)
y_grid(j)];
                    g(max(c)+1).radius          = [0];
                    g(max(c)+1).birthday        = t(1);

                    c(j,1)                      = max(c)+1;

          end
        end




        % DATA EXPORT TO COMSOL
        % generate interpolation function for c, which may be
interpolated back
        % onto COMSOL xy
        % Use 'nearestinterp' for c interpolation because c is
discrete.
        c_interp   = fit([x_grid y_grid], c, 'nearestinterp');


        t_track    = [t_track max(t)];
```

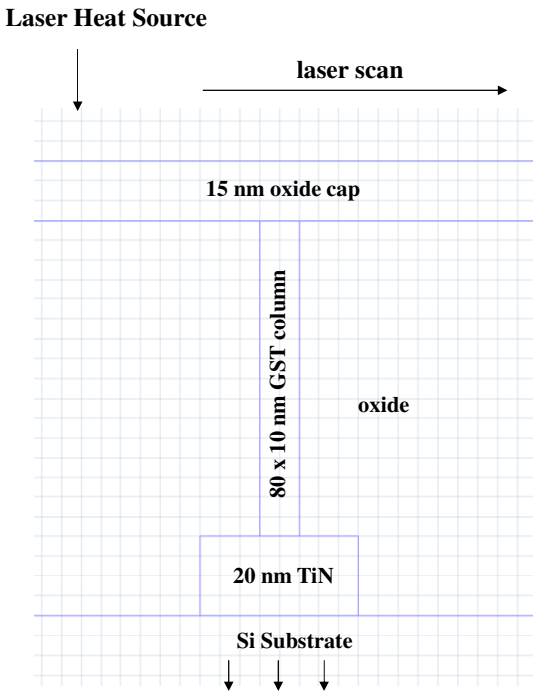
```
        % setting t_previous to current time for the next unique
timestep
        t_previous = t(1);

        % compiling c-map results for each timestep
        c_results = [c_results c];


        % setting up data banks for next timestep
        bank(length(t_track)).x = [];
        bank(length(t_track)).y = [];
        bank(length(t_track)).T = [];
        bank(length(t_track)).t = [];

        % clearing the bank to prevent large loading times
        bank(length(t_track)-1).x = [];
        bank(length(t_track)-1).y = [];
        bank(length(t_track)-1).T = [];
        bank(length(t_track)-1).t = [];
    end

    % For non-unique timesteps, x-y data must be accumulated into the
bank
    if  (t(1) == t_previous)
        bank(length(t_track)).x = [bank(length(t_track)).x; x];
        bank(length(t_track)).y = [bank(length(t_track)).y; y];
        bank(length(t_track)).T = [bank(length(t_track)).T; T];
        bank(length(t_track)).t = [bank(length(t_track)).t; t(1)];
    end

    c_interp   = fit([x_grid y_grid], c, 'nearestinterp');


save('R:\DCM\DCMn.mat','t_track','t_previous','delta_t','c','g','c_resu
lts','bank','-v6');

    % Interpolate random data back onto COMSOL x,y.
    % Note that the size of COMSOL x,y varies with time.
    % Interpolation can lead to c outside of desired range
    % Use logic statements to clip c to fall within desired range.
%     z = c_interp(x,y);
else

    % If R = 1, then only load previous result and do not run function
    load('R:\DCM\DCMn.mat');
    [idx idx] = min(abs(t_track - t(1)));
    c_interp   = fit([x_grid y_grid], c_results(:,idx),
'nearestinterp');

end

% output interpolated c map onto COMSOL xy space
out = c_interp(x,y);
```

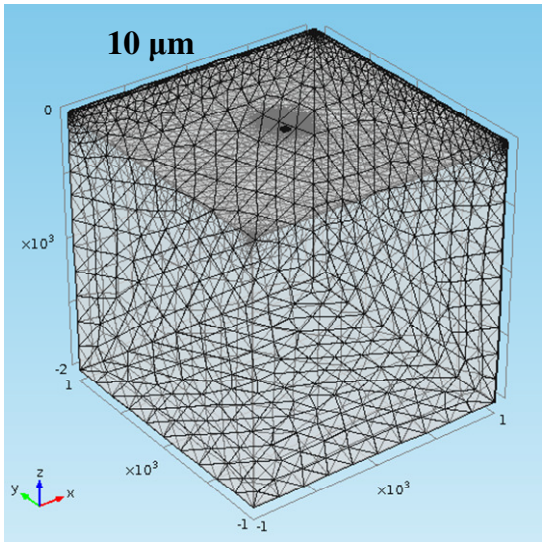
DCM0.mat initialization variables:

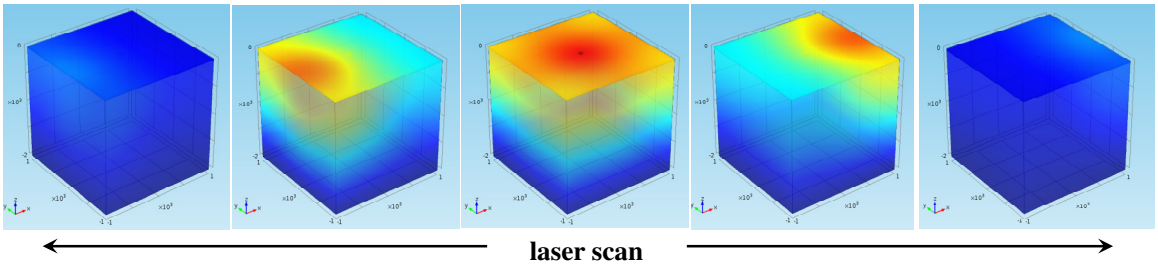
Name	Value	Min	Max
c_interp	[ ]		
count	0	0	0
delta_t	0	0	0
g	<1x1 struct>		
t_previous	0	0	0
t_track	0	0	0

8.3 MATLAB crystallization model results

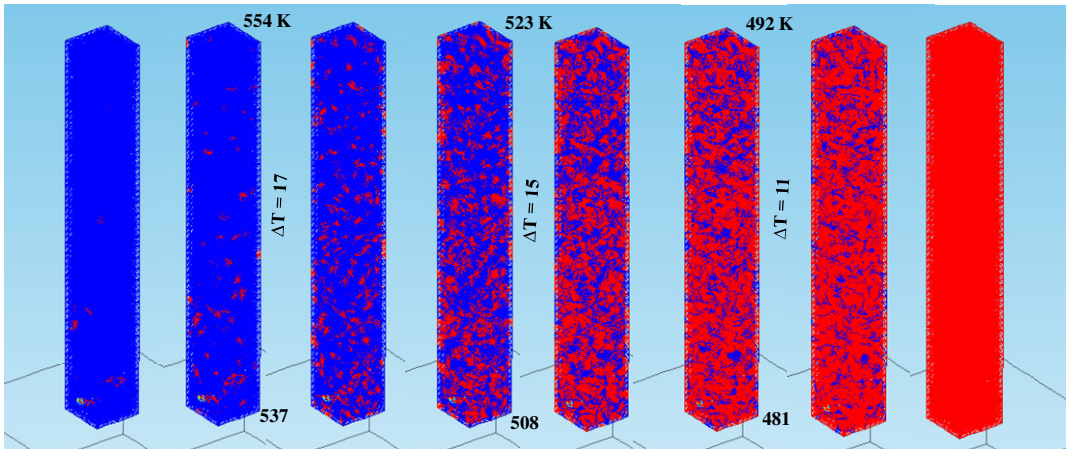
The MATLAB-COMSOL crystallization model as discussed in Section 5.1 and Appendix 8.2 is used to analyze the effect of laser scan speed on the crystallization pattern in a GST structure. These results are from the 3-D implementation of the function. Here, an 80 nm x 10 nm x 10 nm rectangular GST structure is used for simplicity in the MATLAB arrays. The total simulation volume is a 10 µm x 10 µm x 10 µm cube. A laser with a Gaussian distribution in power with 1 µm standard deviation of the spot size is scanned across the simulation area at various scan speeds. Power for each scan is adjusted such that the temperature is sufficient to melt the entire GST structure while the laser is directly above the cell. Due to the rate of heat diffusion, significant differences in temperature gradients during the scan are observed, and thus differences in the crystallization patterns are also observed. Faster scan rates result in less temperature gradient and more uniform crystallization, whereas slower scan rates have higher temperature gradients and begin crystallization from one end of the structure due to the strong temperature dependence of the nucleation and growth rates.



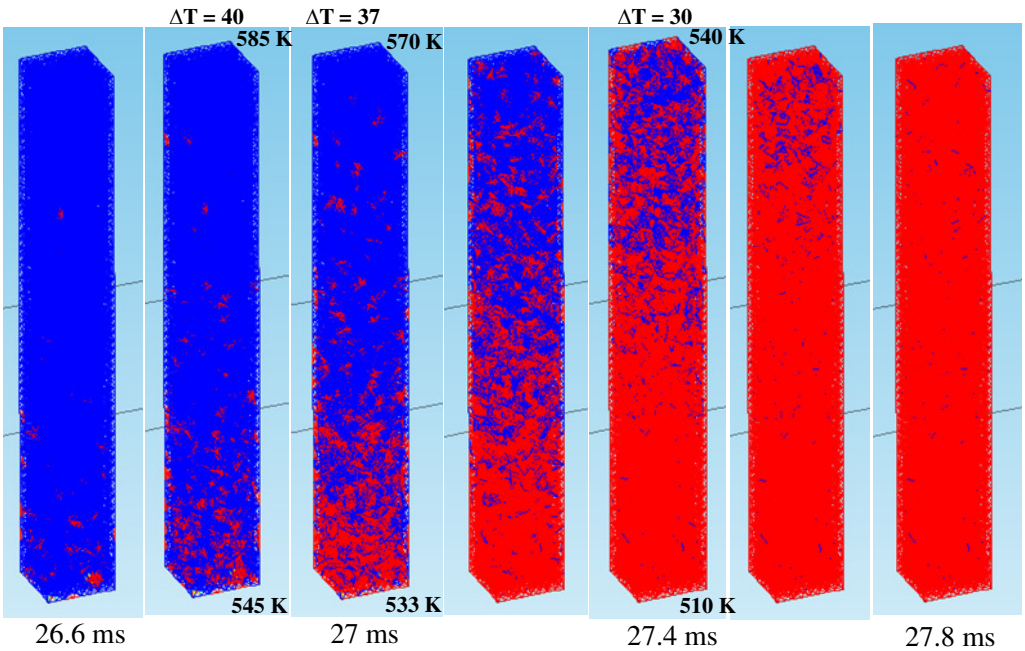




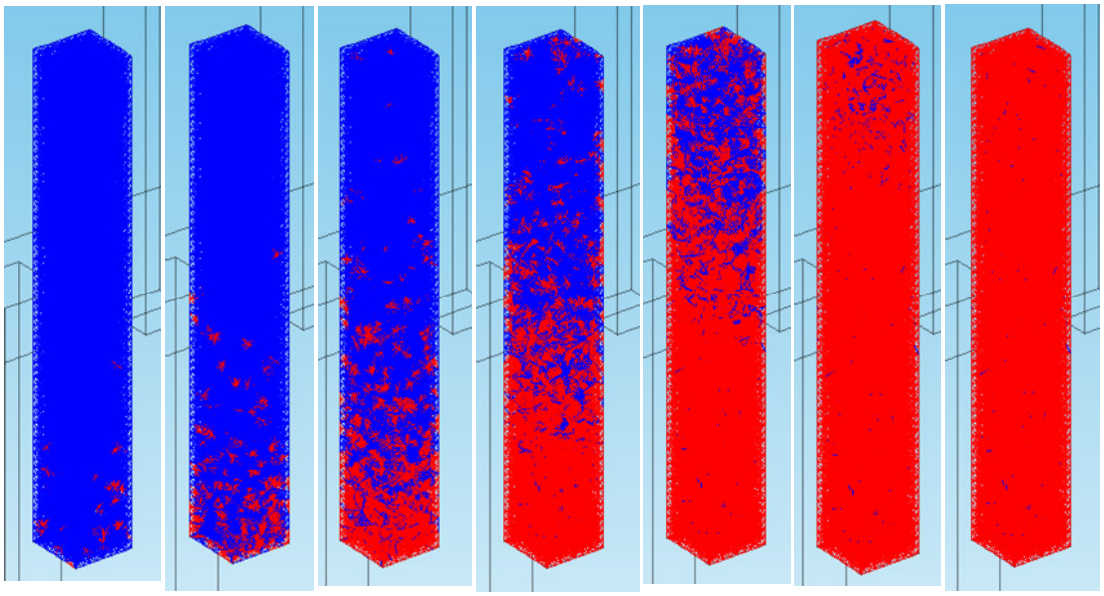
Scan speed: 1.25 mm/s, Simulation time 0 to 4 ms, Peak melting temp at 2 ms



Scan speed: 0.125 mm/s
Simulation time 0 to 40 ms
Peak melting temp at 20 ms



Scan speed: 0.0125 mm/s, Simulation time 0 to 400 ms, Peak melting temp at 200 ms

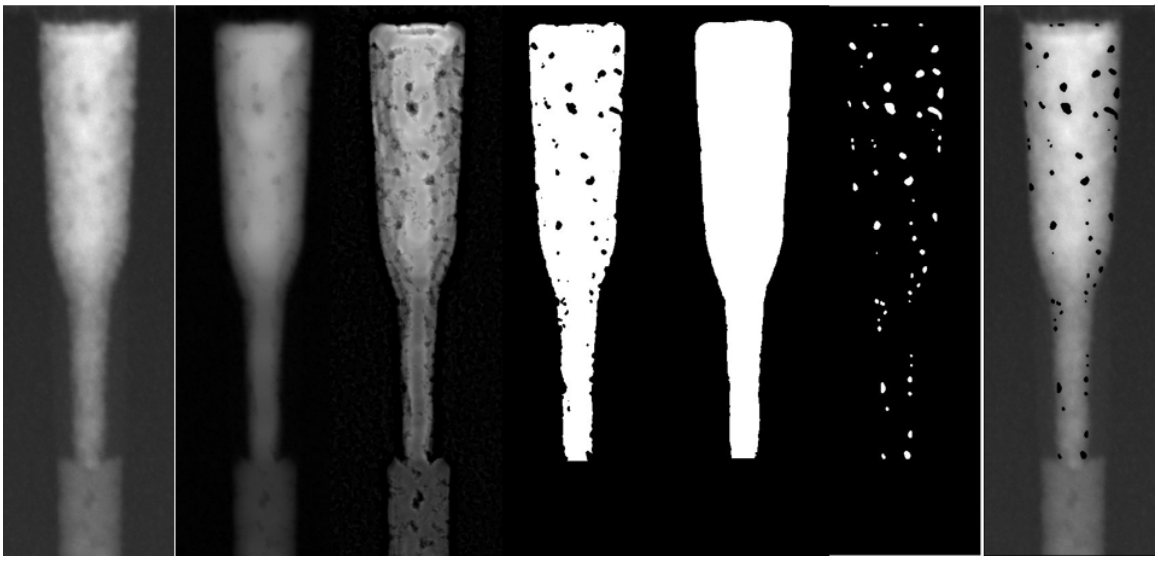


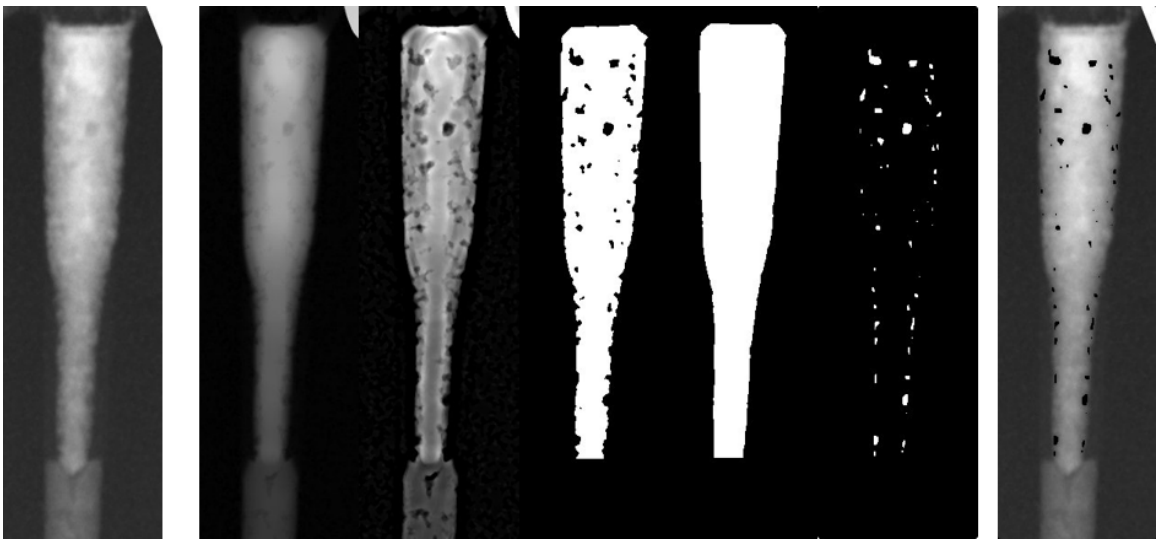
264 ms 266 ms 268 ms 270 ms 272 ms 274 ms 276 ms

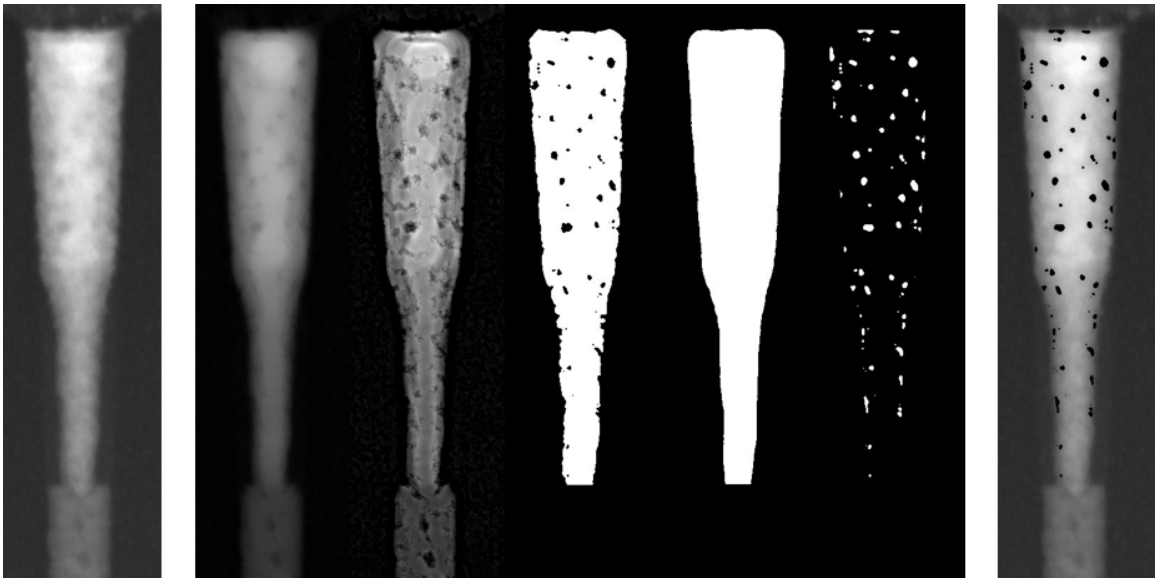
8.4 Image processing technique for void area estimation

Image J software is used. Images/techniques from left to right are: Original image, subtract background +remove outliers, unsharp mask, local threshold, threshold, difference between threshold and local threshold, highlighted void areas imposed on the original image.

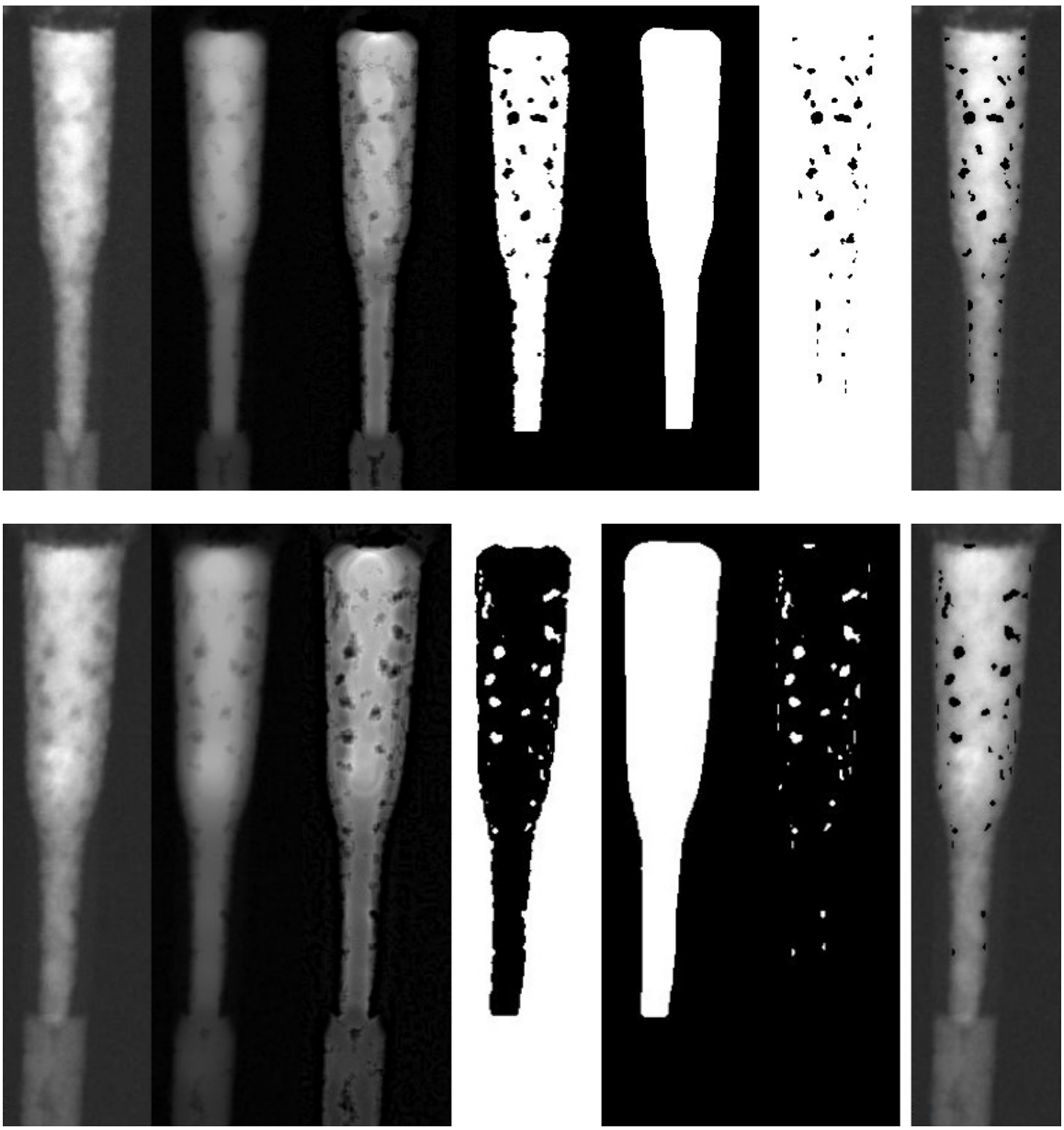
1x scan case:







5X scan case:



8.5 GST Nanostructure fabrication steps

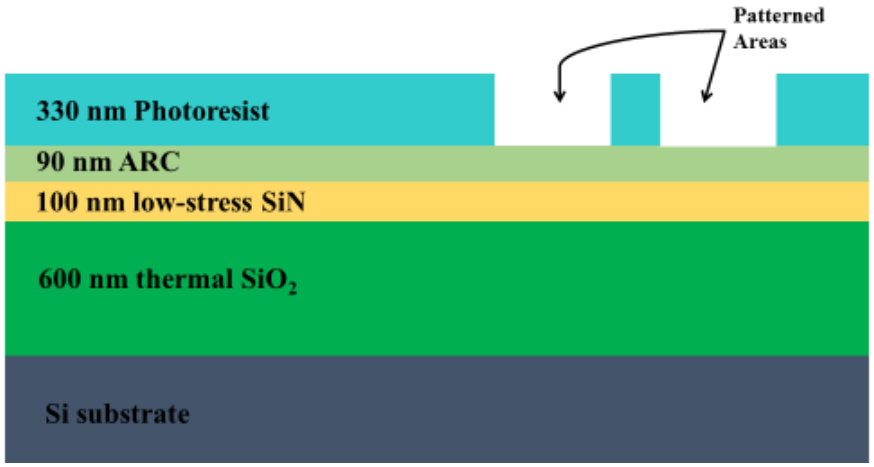
Fabrication process steps for PCMUCONI2L41 lot at the Microelectronics Research Laboratory at the IBM Thomas J. Watson Research Center are shown below. The process steps are named according to the Microelectronics Research Laboratory. 2-D cross section diagrams of the wafers are shown below each group of steps to illustrate the results of the process steps.

1. CONTROL	Pull wafers
2. CONTROL	Record Wafer IDs / Attach Wafer ID Map
3. FEOL-WETS	OZONE HUANG CLEAN
4. FEOL-WETS	SPIN,RINSE AND DRY

5. HOT	THICK OXIDE
6. HOT	MEASURE Tox
7. HOT	THICK OXIDE
8. FILMS 1-2	480C Low Stress Nitride H450A
9. FILMS 1-2	thickness measurement on 7-2 Rudoloph
10. FILMS 1-2	480C Low Stress Nitride H450A
11. FEOL-WETS	OZONE MOD HUANG CLEAN (NO DHF)
12. FEOL-WETS	SPIN,RINSE AND DRY

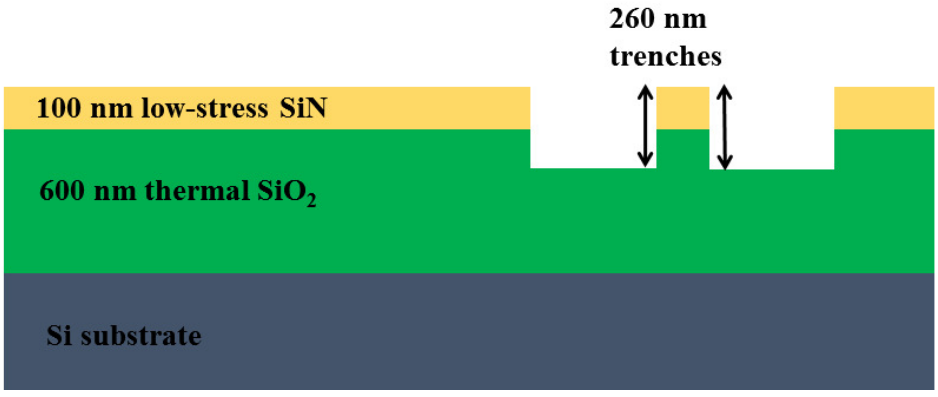
13. LITH 193	TRANSFER WAFERS TO AISLE 31
14. LITH 193	AR40 + JSR AM-2073
15. LITH 193	193 ASML EXPOSURE
16. LITH 193	TRANSFER WAFERS TO 7-2 Lab
17. METROLOGY	JEOL SEM Inspection
18. TEST-INIT	1.5-hr test

19. LITH 193	TRANSFER WAFERS TO AISLE 31
20. LITH 193	AR40 + JSR AM-2073
21. LITH 193	193 ASML EXPOSURE
22. LITH 193	TRANSFER WAFERS TO 7-2 Lab
23. METROLOGY	JEOL SEM Inspection
24. TEST-INIT	1.5-hr test



25. RIE 8-2	8-2 Ingating for Engineering attention
26. RIE 8-2	Y56A DPS II Cold Cathode Experimental
27. RIE 8-2	Y56D Enabler Experimental
28. RIE 8-2	Y58 P-15 Profilometry (No Metals) Tencor 7-2
29. METROLOGY	JEOL SEM Inspection
30. TEST-INIT	1.5-hr test
31. LITH DUV	O2 plasma Gasonics
32. FEOL-WETS	Sulfuric Nitric Clean 10mins, remove organics
33. FEOL-WETS	SPIN,RINSE AND DRY
34. TEST-INIT	1.5-hr test

35. RIE 8-2	Y56A DPS II Cold Cathode Experimental
36. RIE 8-2	Y56D Enabler Experimental
37. RIE 8-2	Y58 P-15 Profilometry (No Metals) Tencor 7-2
38. METROLOGY	JEOL SEM Inspection
39. TEST-INIT	1.5-hr test
40. LITH DUV	O2 plasma Gasonics
41. FEOL-WETS	Sulfuric Nitric Clean 10mins, remove organics
42. FEOL-WETS	SPIN,RINSE AND DRY
43. FEOL-WETS	OZONE MOD HUANG CLEAN (NO DHF)
44. FEOL-WETS	SPIN,RINSE AND DRY

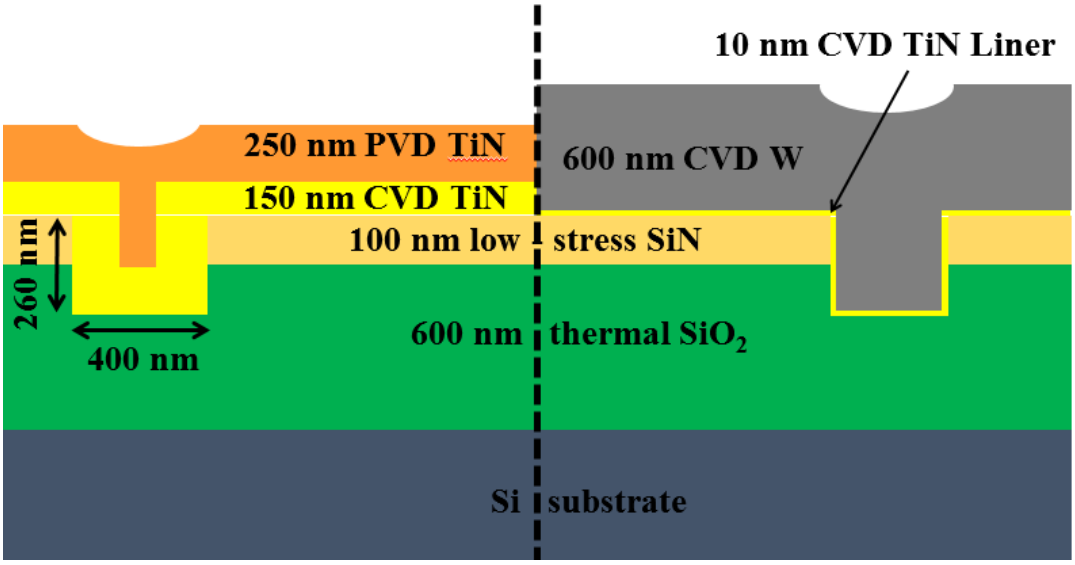


W# 2, 4, 6, 8, 9

45. METAL 1-2 wafer transport to 1-2
46. METAL 1-2 CVD TiN optional sputter-clean
47. METAL 1-2 CVD TiN optional sputter-clean
48. METAL 1-2 TiN PVD POR

W# 1, 3, 5, 7

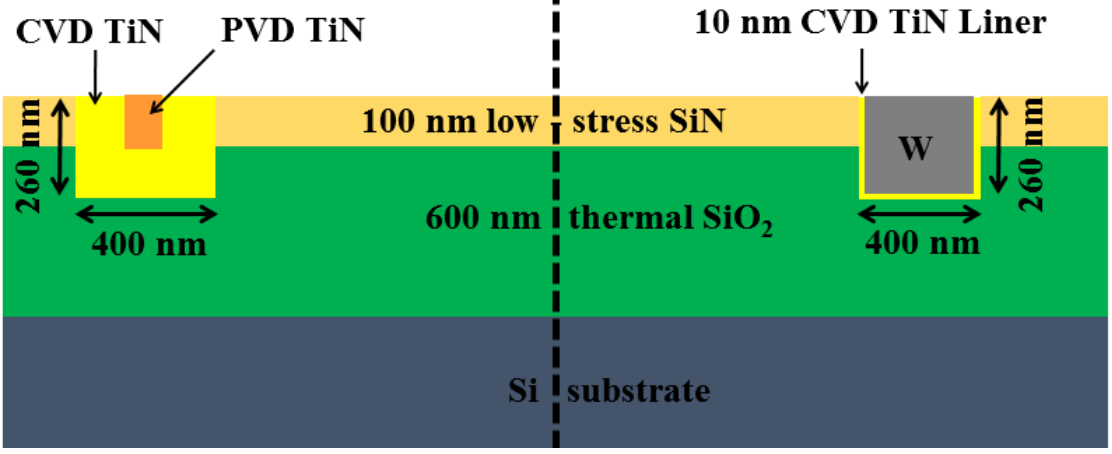
49. METAL 1-2 CVD TiN optional sputter-clean
50. METAL 1-2 wafer transport to 7-2 in gating
51. METAL 7-2 Sequence: W_395C_Si5_06K



53. POLISH Pre CMP-Process Developmen-Transport to CMP lab
54. POLISH W CMP
55. POLISH CMP ONLY//ONTRAK Brush Clean for MOL
56. POLISH LEICA Optical Inspection (Westech)
57. POLISH W Liner CMP
58. POLISH CMP ONLY//ONTRAK Brush Clean for MOL
59. POLISH LEICA Optical Inspection (Westech)
60. TEST-INIT 1.5-hr test
61. POLISH PCM Development CMP for TiN polish
62. POLISH CMP ONLY//ONTRAK Brush Clean for MOL
63. POLISH LEICA Optical Inspection (Westech)
64. POLISH Post Measurement - Transport to 7-2 Changeroom

W# 2, 4, 6, 8, 9

W# 1, 3, 5, 7

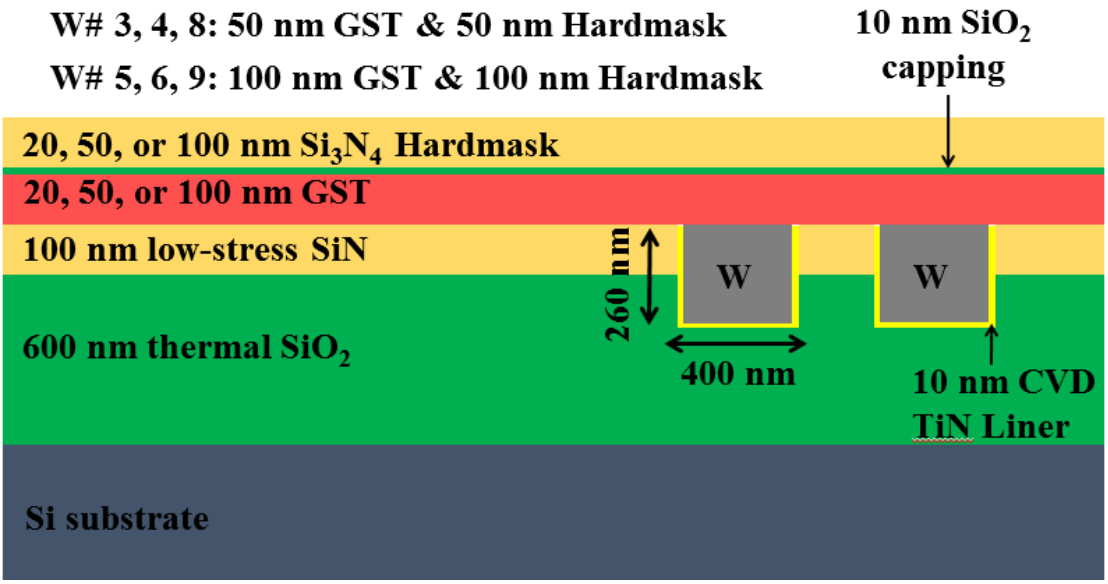


65. TEST-INIT	Initiator Coordination (GST dep.)	71. DIEL 1-2	200C nitride no NH3 pretreatment H450C
66. DIEL 1-2	Wafer transport to aisle 1-2 from 7-2	72. DIEL 1-2	thickness measurement on Rudolph
67. DIEL 1-2	200C nitride no NH3 pretreatment H450C	73. DIEL 1-2	200C nitride no NH3 pretreatment H450C
68. DIEL 1-2	thickness measurement on Rudolph	74. DIEL 1-2	200C nitride no NH3 pretreatment H450C
69. DIEL 1-2	200C nitride no NH3 pretreatment H450C	75. DIEL 1-2	200C nitride no NH3 pretreatment H450C
70. DIEL 1-2	thickness measurement on Rudolph	76. DIEL 1-2	Wafer transport to 7-2 from 1-2

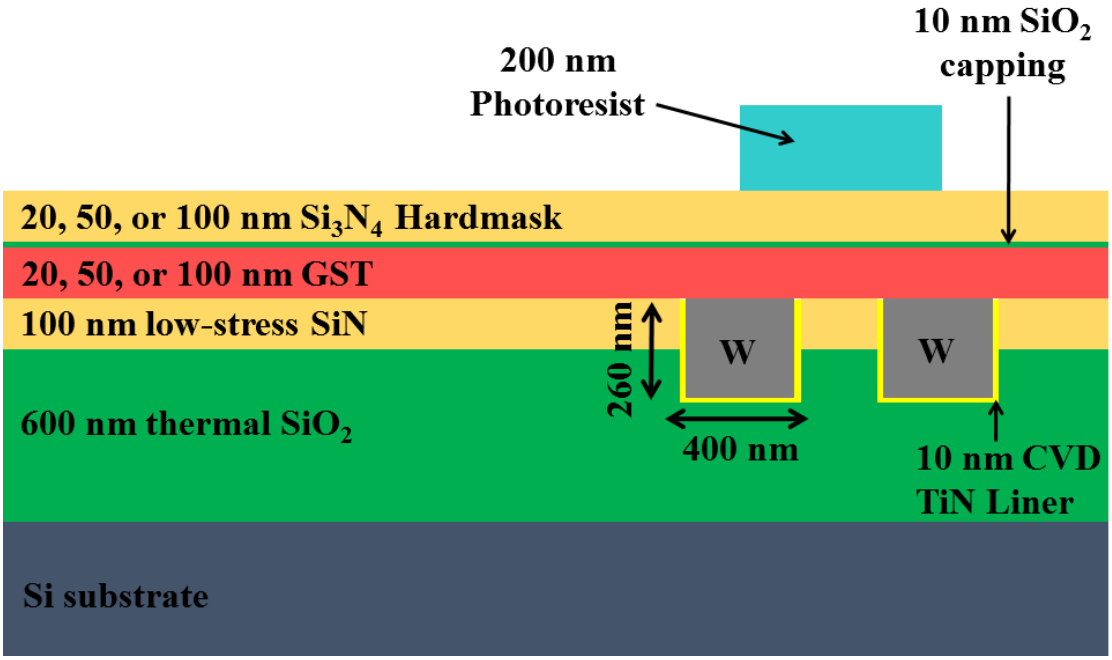
W# 1, 2, 7: 20 nm GST & 20 nm Hardmask

W# 3, 4, 8: 50 nm GST & 50 nm Hardmask

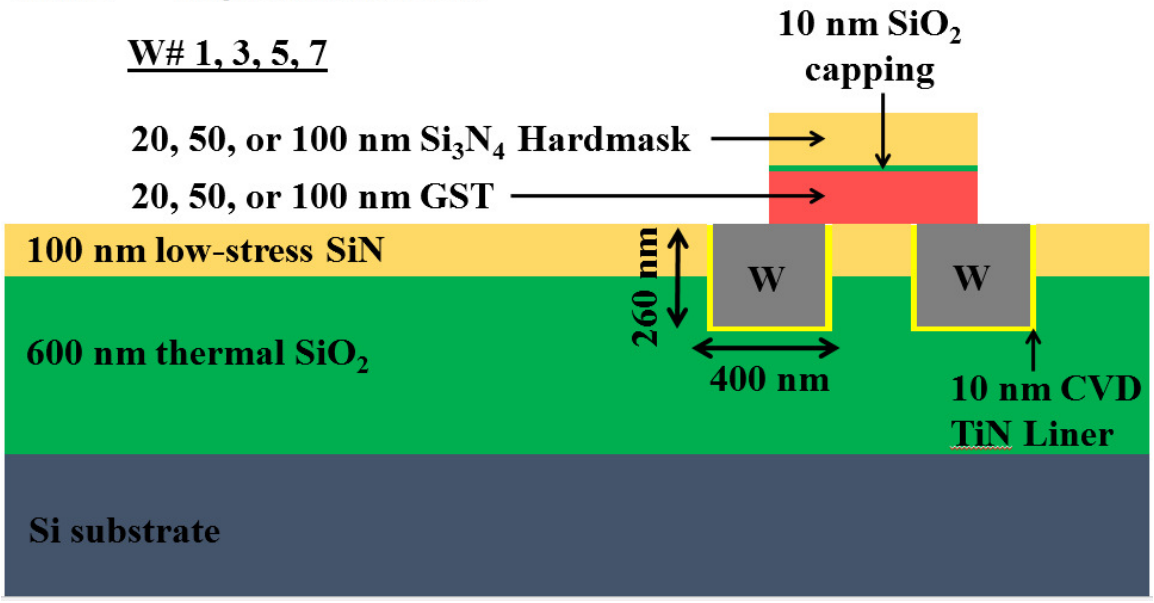
W# 5, 6, 9: 100 nm GST & 100 nm Hardmask

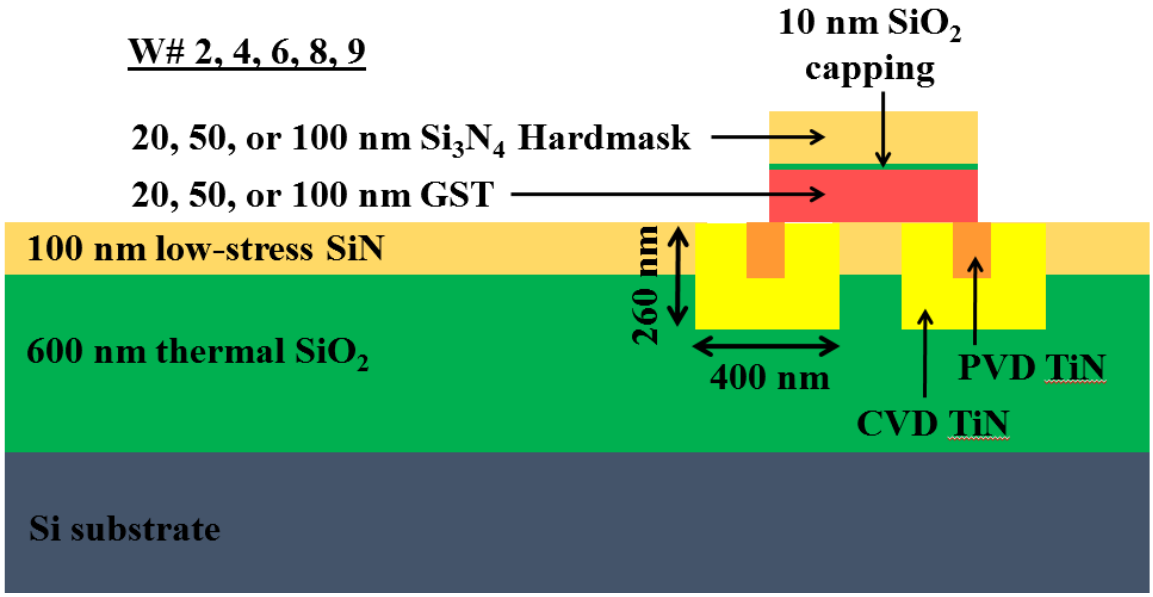


77. LITH 193	TRANSFER WAFERS TO AISLE 31	81. METROLOGY	JEOL SEM Inspection
78. LITH 193	5Gate RX - Integrated	82. TEST-INIT	1.5-hr test
79. METROLOGY	Q7 OVERLAY MEASURE with Mean Plus 2-Sigma	83. LITH 193	TRANSFER WAFERS TO AISLE 31
80. METROLOGY	TRANSFER WAFERS TO 7-2	84. LITH 193	5Gate RX - Integrated
		85. LITH 193	TRANSFER WAFERS TO 7-2 Lab



86. RIE 5-2	Ingating for Engineering attention
87. RIE 5-2	Y14PM1 - 9400 Experimental
88. RIE 5-2	Y14PM1 - 9400 Experimental
89. RIE 5-2	Transport Wafers from 5-2 TO 11-2
90. RIE 11-2	Y223C High Temp Downstream PR STRIP
91. TEST-INIT	1.5-hr test
92. RIE 5-2	Ingating for Engineering attention
93. RIE 5-2	Y14PM1 - 9400 Experimental
94. RIE 5-2	Y14PM1 - 9400 Experimental
95. RIE 5-2	Transport Wafers from 5-2 TO 11-2
96. RIE 11-2	Y223C High Temp Downstream PR STRIP
97. TEST-INIT	1.5-hr test
98. RIE 5-2	Ingating for Engineering attention
99. RIE 5-2	Y14PM1 - 9400 Experimental
100. RIE 5-2	Y14PM1 - 9400 Experimental
101. RIE 5-2	Transport Wafers from 5-2 TO 11-2
102. RIE 11-2	Y223C High Temp Downstream PR STRIP
103. TEST-INIT	1.5-hr test
104. COMPLETED	Return Wafers to Initiator





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